FIG. 1

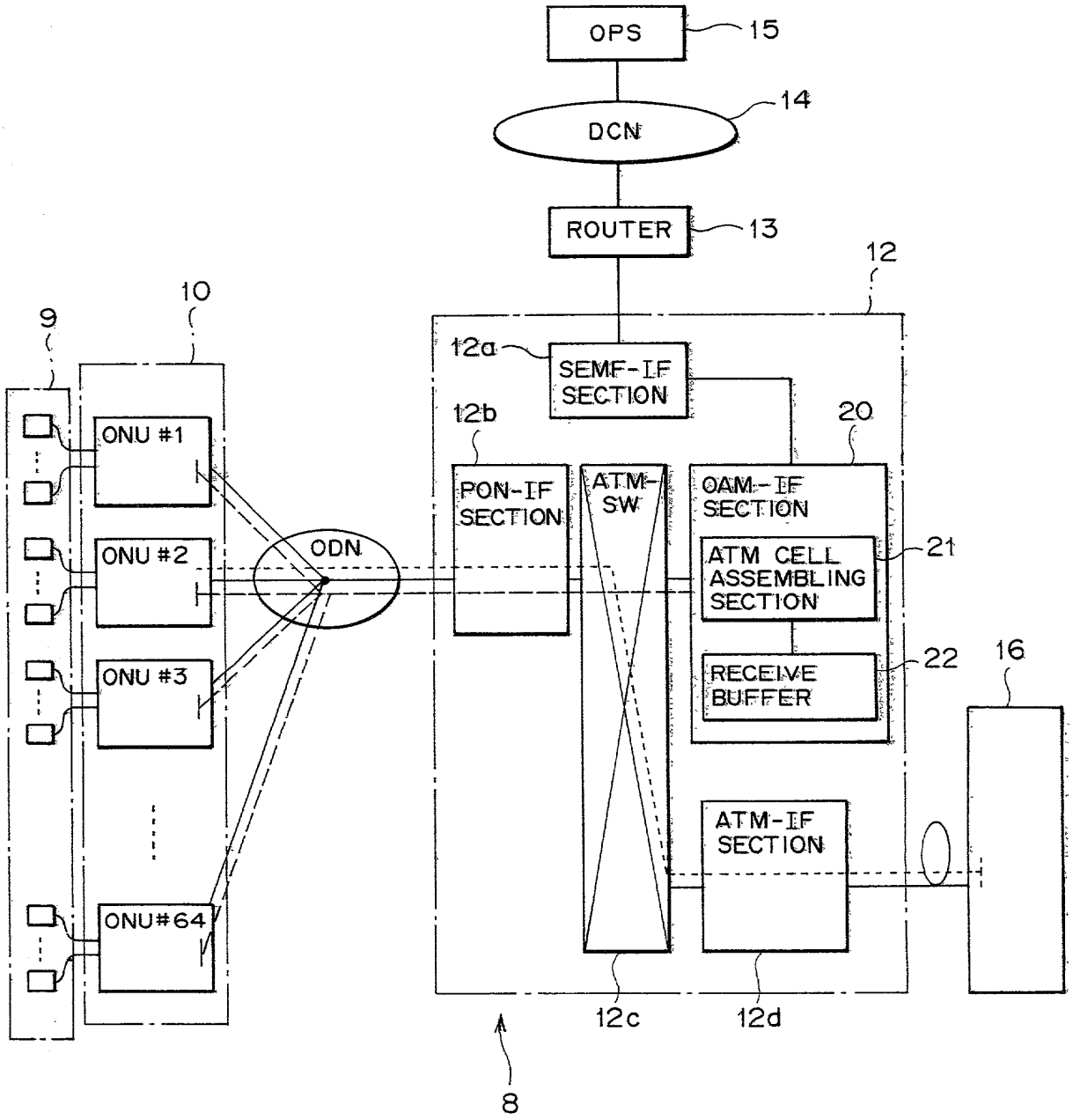
OPS
15
DCN
14
ROUTER
13
12
10
9
12a
SEMF-IF SECTION
12b
20
PON-IF SECTION
ATM-SW
OAM-IF SECTION
ATM CELL ASSEMBLING SECTION
21
RECEIVE BUFFER
22
16
ATM-IF SECTION
ONU #1
ONU #2
ONU #3
ONU#64
ODN
12c
12d
8

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FIG. 2

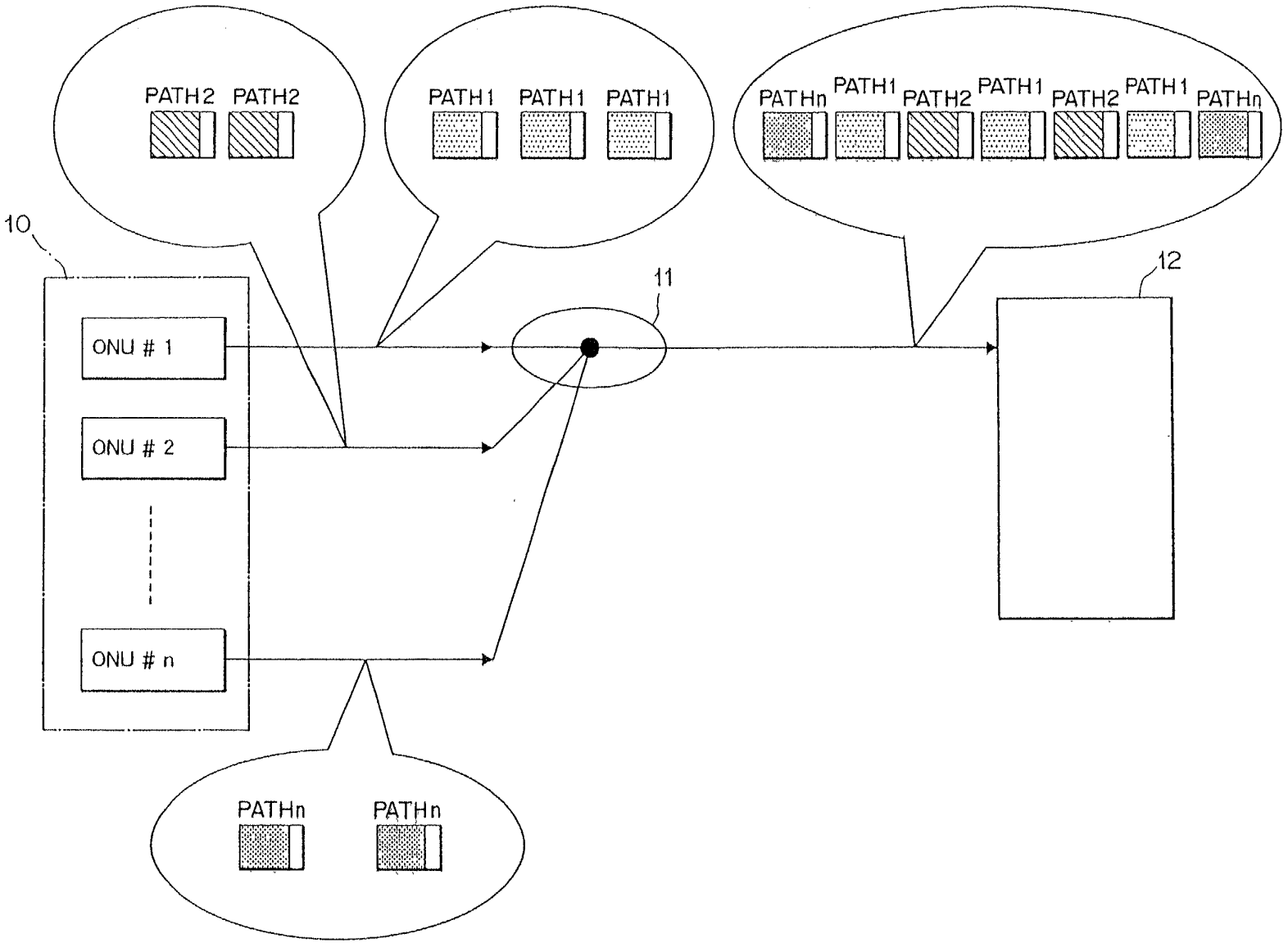

FIG. 3

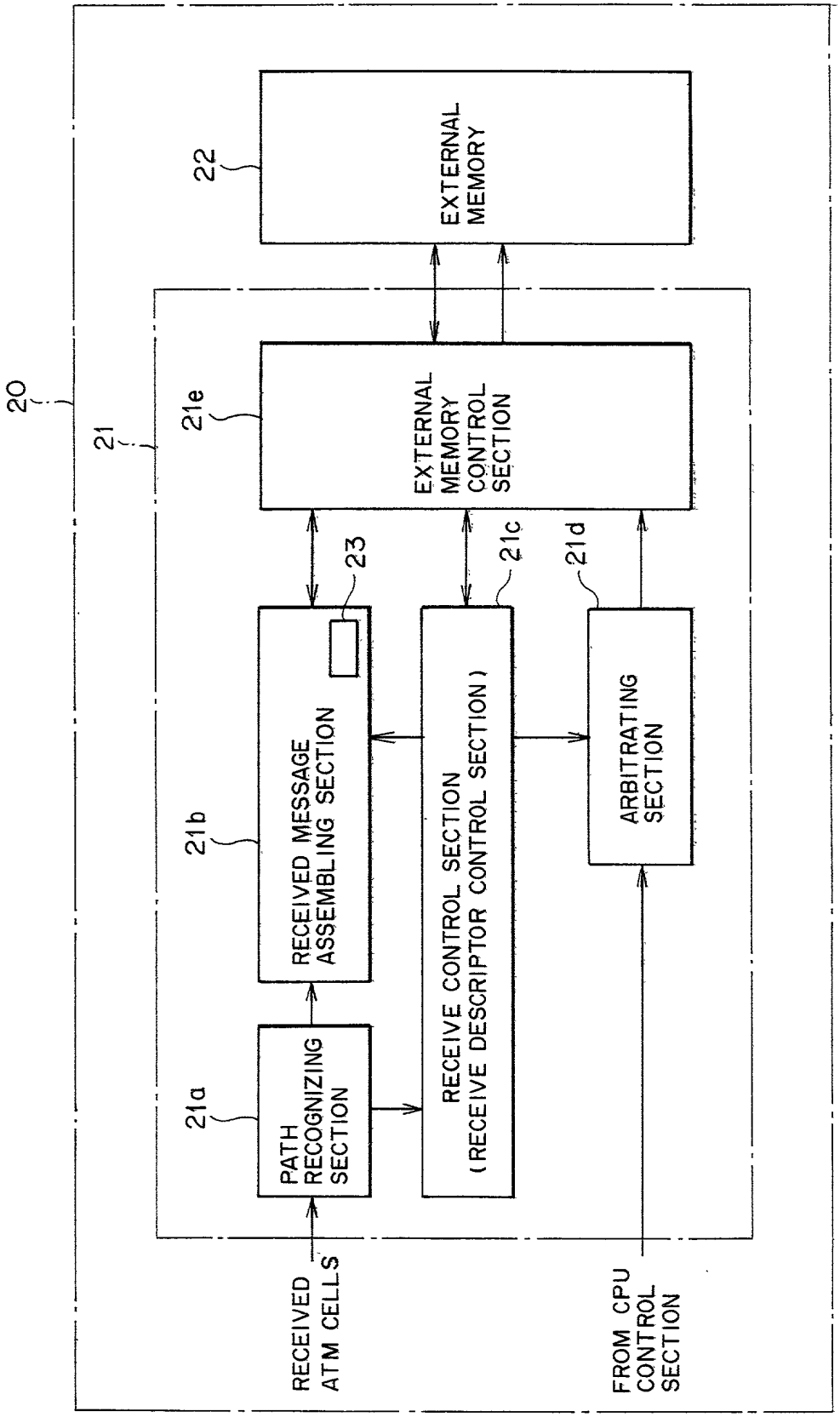
20
21
22
EXTERNAL MEMORY
21e
EXTERNAL MEMORY CONTROL SECTION
23
21c
21d
21b
RECEIVED MESSAGE ASSEMBLING SECTION
RECEIVE CONTROL SECTION (RECEIVE DESCRIPTOR CONTROL SECTION)
ARBITRATING SECTION
21a
PATH RECOGNIZING SECTION
RECEIVED ATM CELLS
FROM CPU CONTROL SECTION

FIG. 4

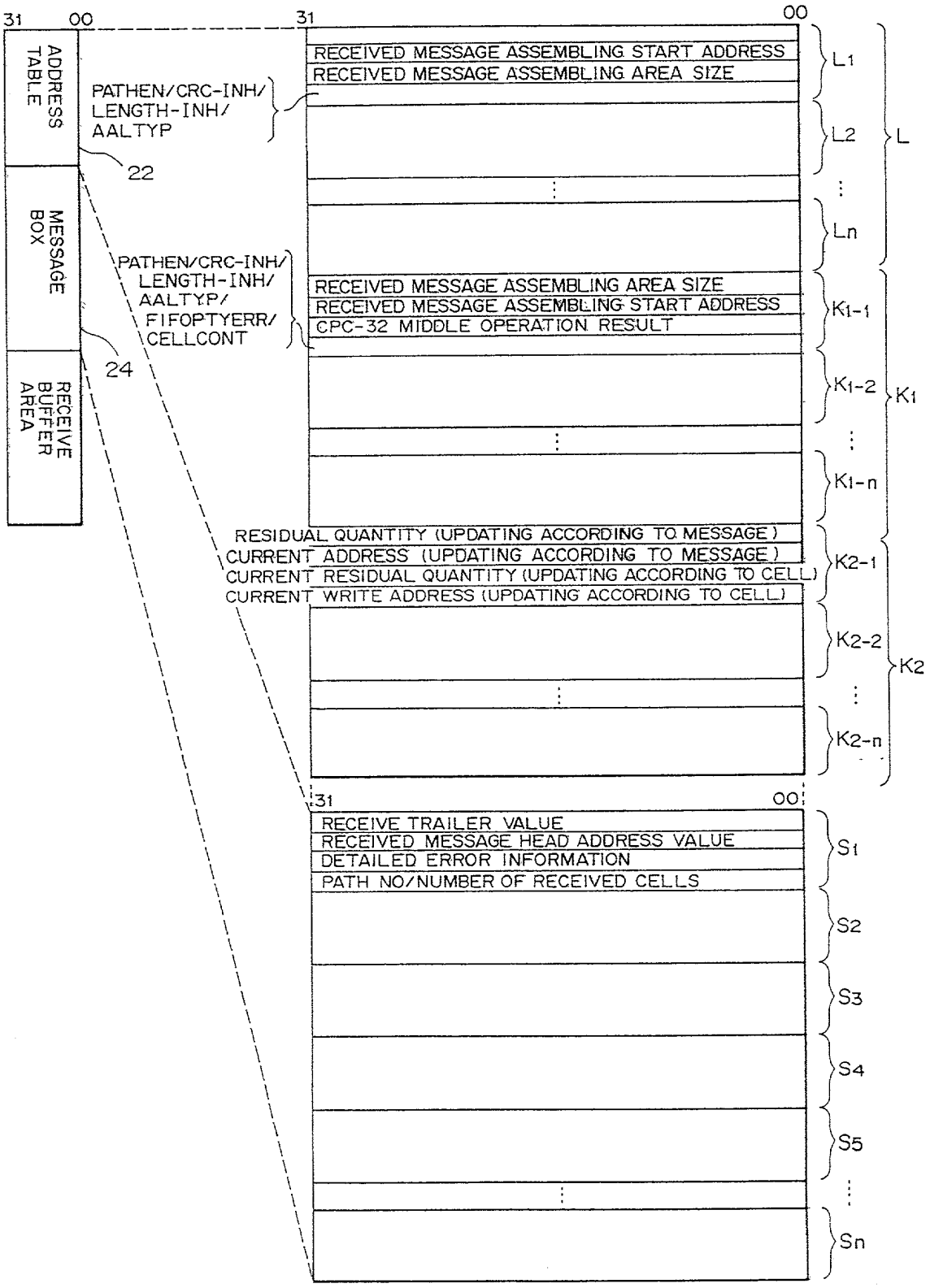
31
00
ADDRESS TABLE
MESSAGE BOX
RECEIVE BUFFER AREA
PATHEN/CRC-INH/
LENGTH-INH/
AALTYP
22
PATHEN/CRC-INH/
LENGTH-INH/
AALTYP/
FIFOPTYERR/
CELLCONT
24
RECEIVED MESSAGE ASSEMBLING START ADDRESS
RECEIVED MESSAGE ASSEMBLING AREA SIZE
RECEIVED MESSAGE ASSEMBLING AREA SIZE
RECEIVED MESSAGE ASSEMBLING START ADDRESS
CPC-32 MIDDLE OPERATION RESULT
RESIDUAL QUANTITY (UPDATING ACCORDING TO MESSAGE)
CURRENT ADDRESS (UPDATING ACCORDING TO MESSAGE)
CURRENT RESIDUAL QUANTITY (UPDATING ACCORDING TO CELL)
CURRENT WRITE ADDRESS (UPDATING ACCORDING TO CELL)
RECEIVE TRAILER VALUE
RECEIVED MESSAGE HEAD ADDRESS VALUE
DETAILED ERROR INFORMATION
PATH NO/NUMBER OF RECEIVED CELLS
L1
L2
Ln
L
K1-1
K1-2
K1-n
K1
K2-1
K2-2
K2-n
K2
S1
S2
S3
S4
S5
Sn

FIG. 5

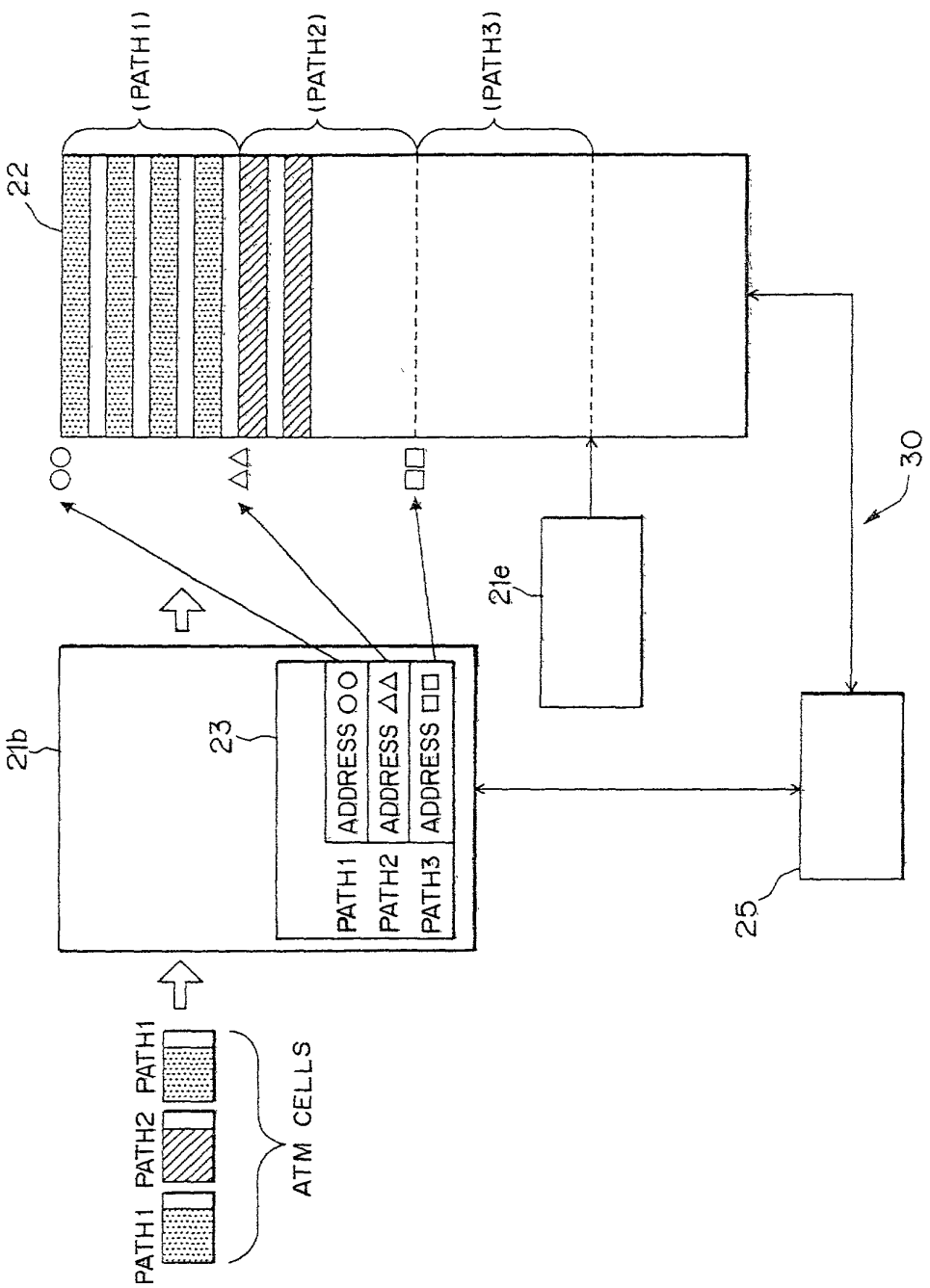
(PATH1)
(PATH2)
(PATH3)
22
○○
△△
□□
30
21e
21b
23
PATH1 ADDRESS ○○
PATH2 ADDRESS △△
PATH3 ADDRESS □□
25
PATH1 PATH2 PATH1
ATM CELLS

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FIG.6

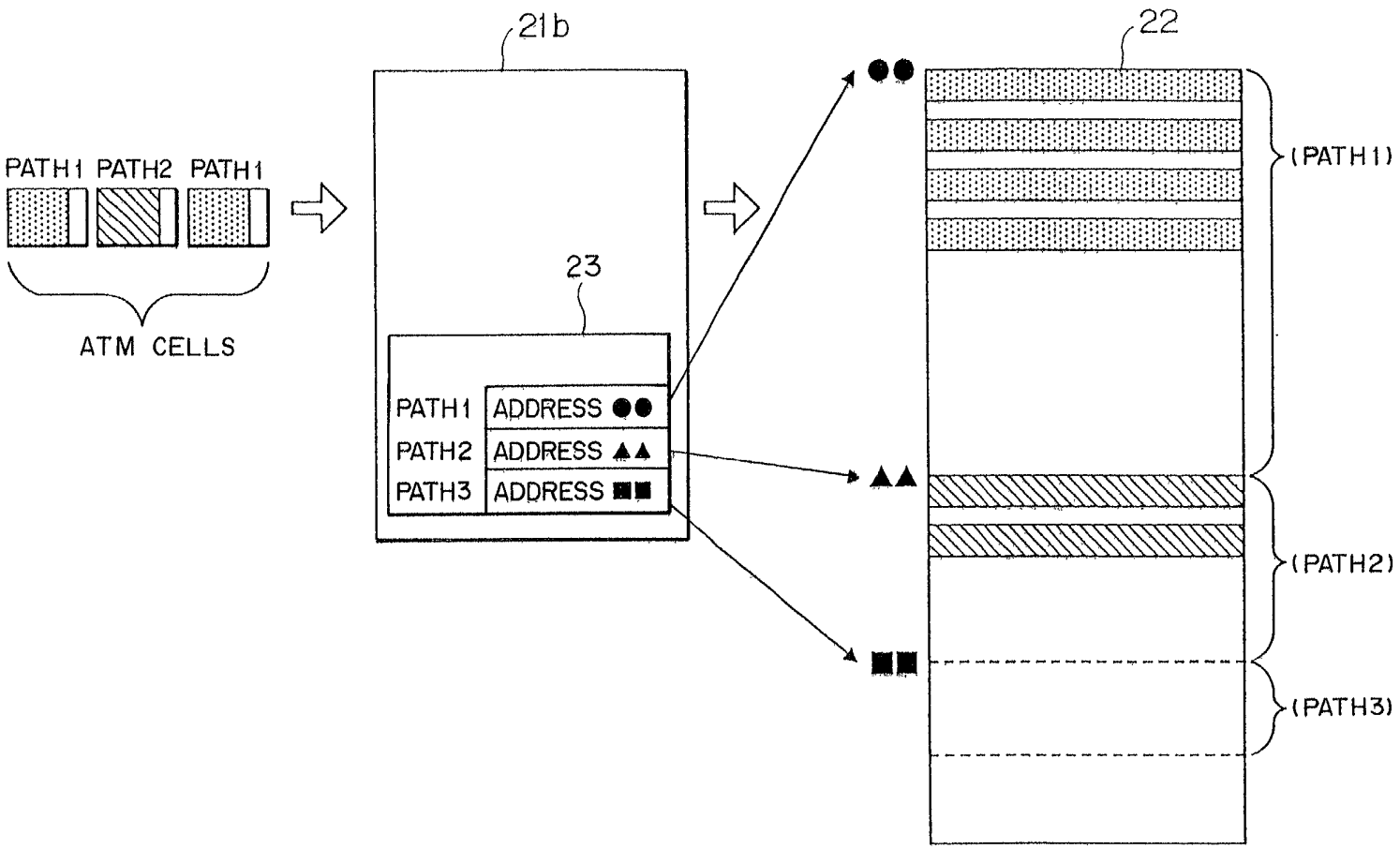


FIG. 7

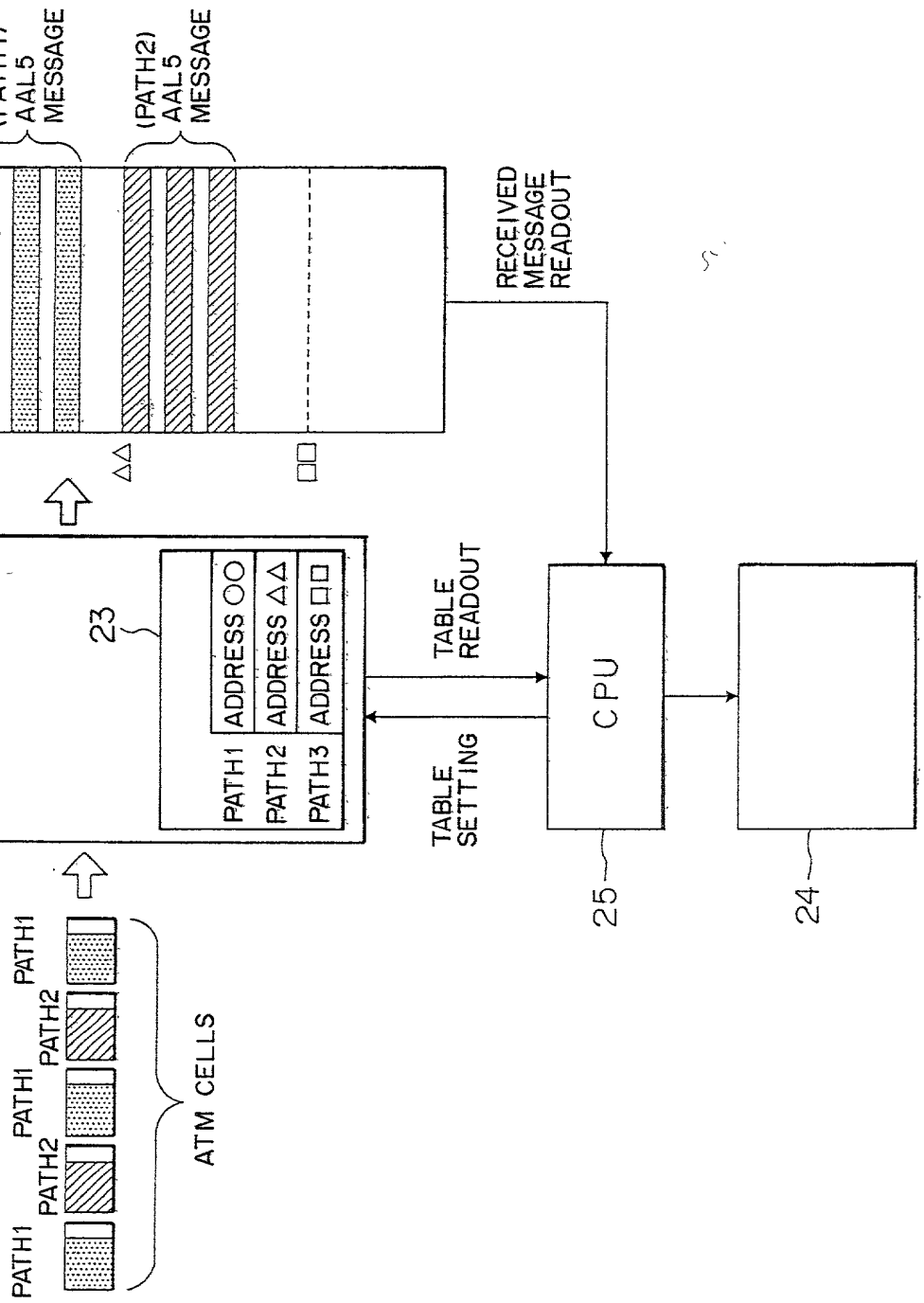

(PATH1) AAL5 MESSAGE
(PATH2) AAL5 MESSAGE
22
○○
△△
□□
RECEIVED MESSAGE READOUT
21b
23
PATH1 ADDRESS ○○
PATH2 ADDRESS △△
PATH3 ADDRESS □□
TABLE READOUT
TABLE SETTING
CPU
25
24
PATH1
PATH2
PATH1
PATH2
PATH1
ATM CELLS

FIG. 8

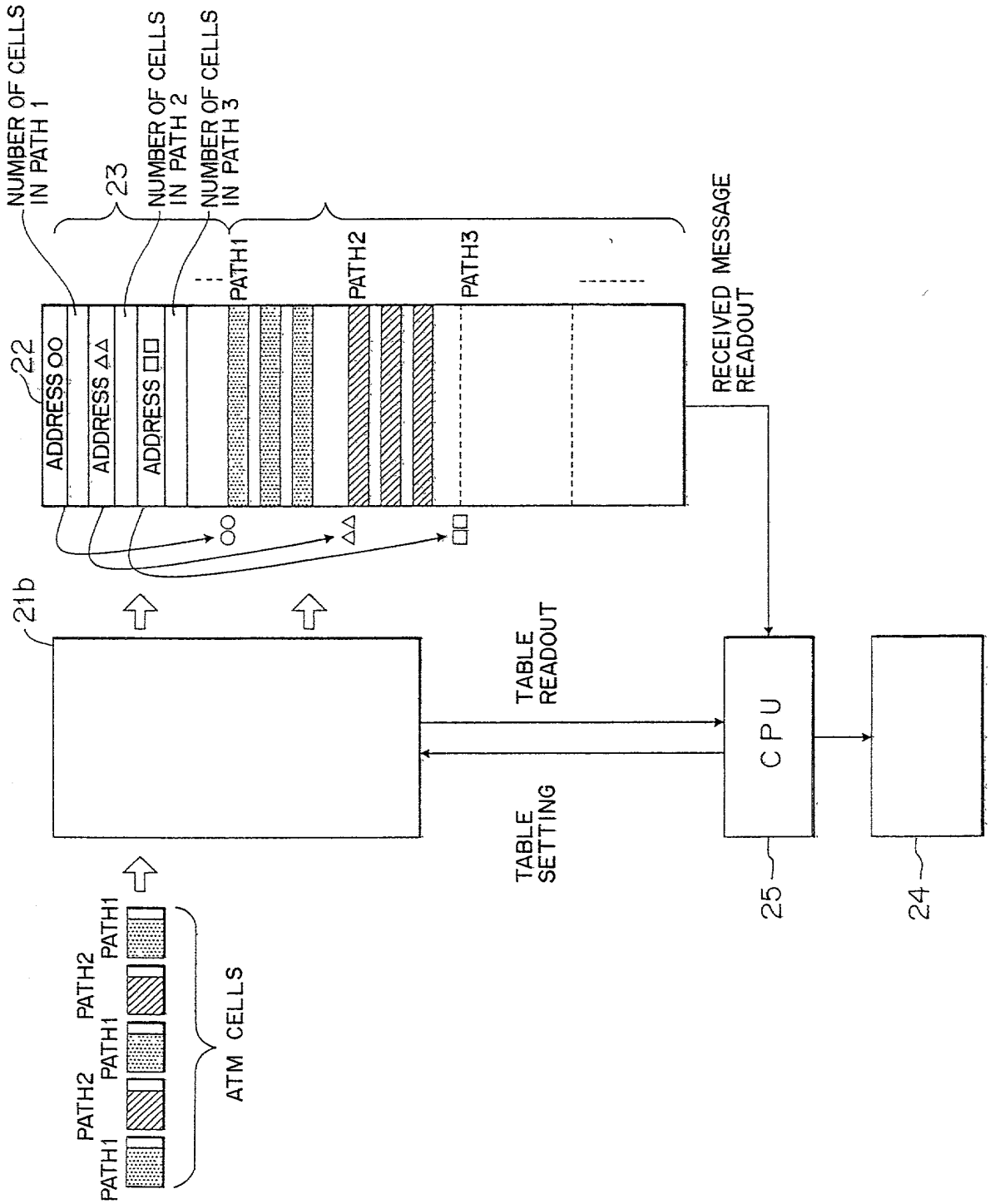

NUMBER OF CELLS IN PATH 1
NUMBER OF CELLS IN PATH 2
NUMBER OF CELLS IN PATH 3
23
22
ADDRESS ○○
ADDRESS △△
ADDRESS □□
PATH1
PATH2
PATH3
RECEIVED MESSAGE READOUT
21b
TABLE READOUT
TABLE SETTING
CPU
25
24
PATH2
PATH1
PATH2
PATH1
PATH1
ATM CELLS

FIG. 9(a)

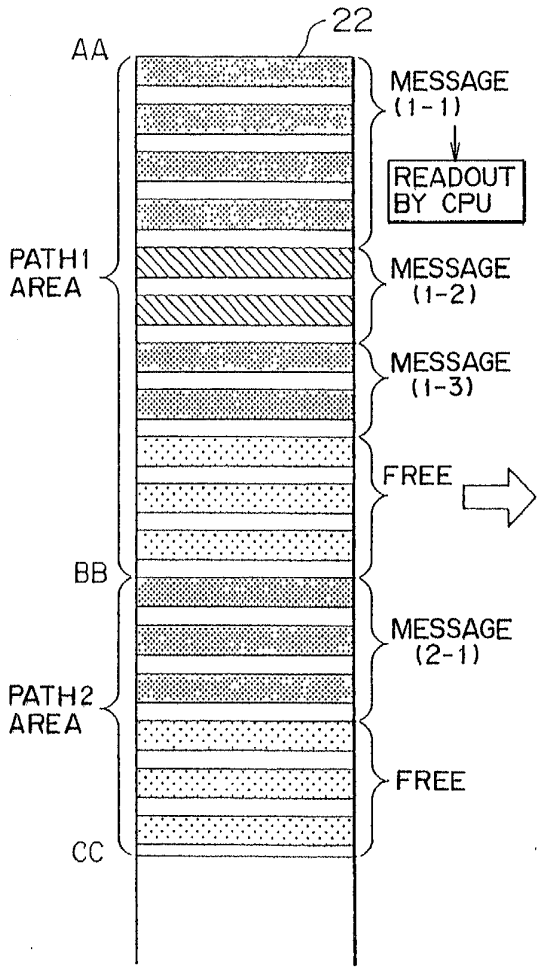


FIG. 9(b)

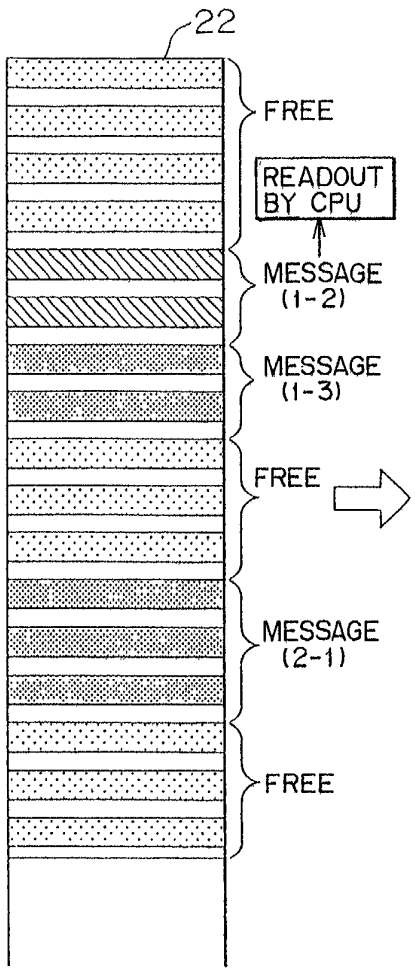


FIG. 9(c)

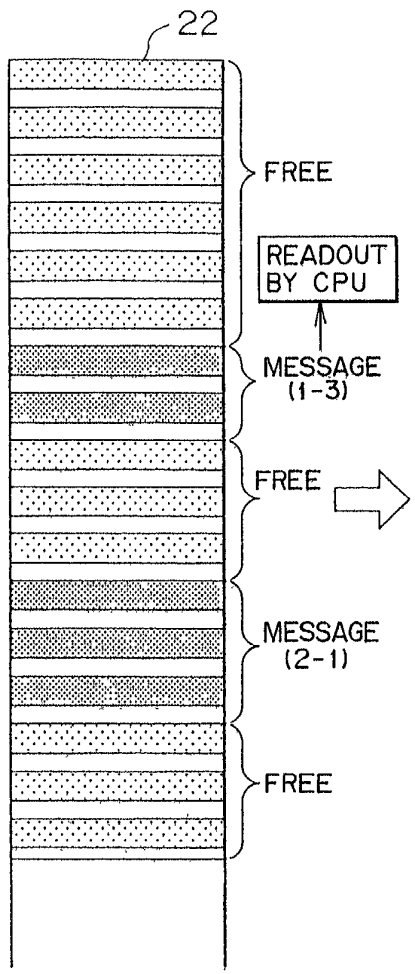


FIG. 9(d)

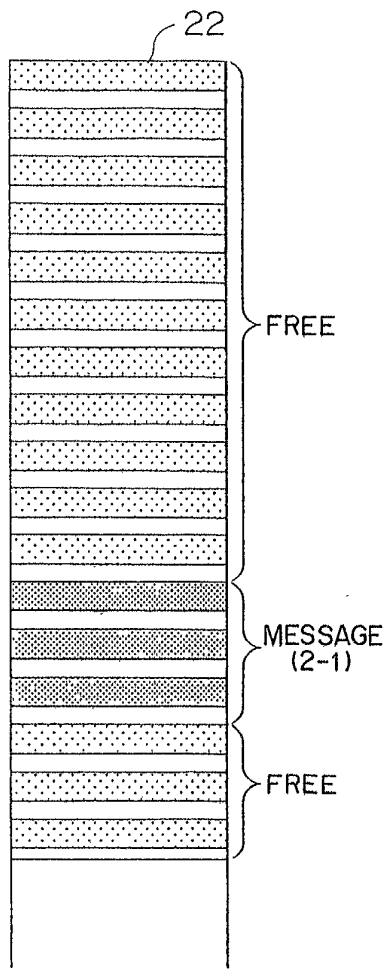
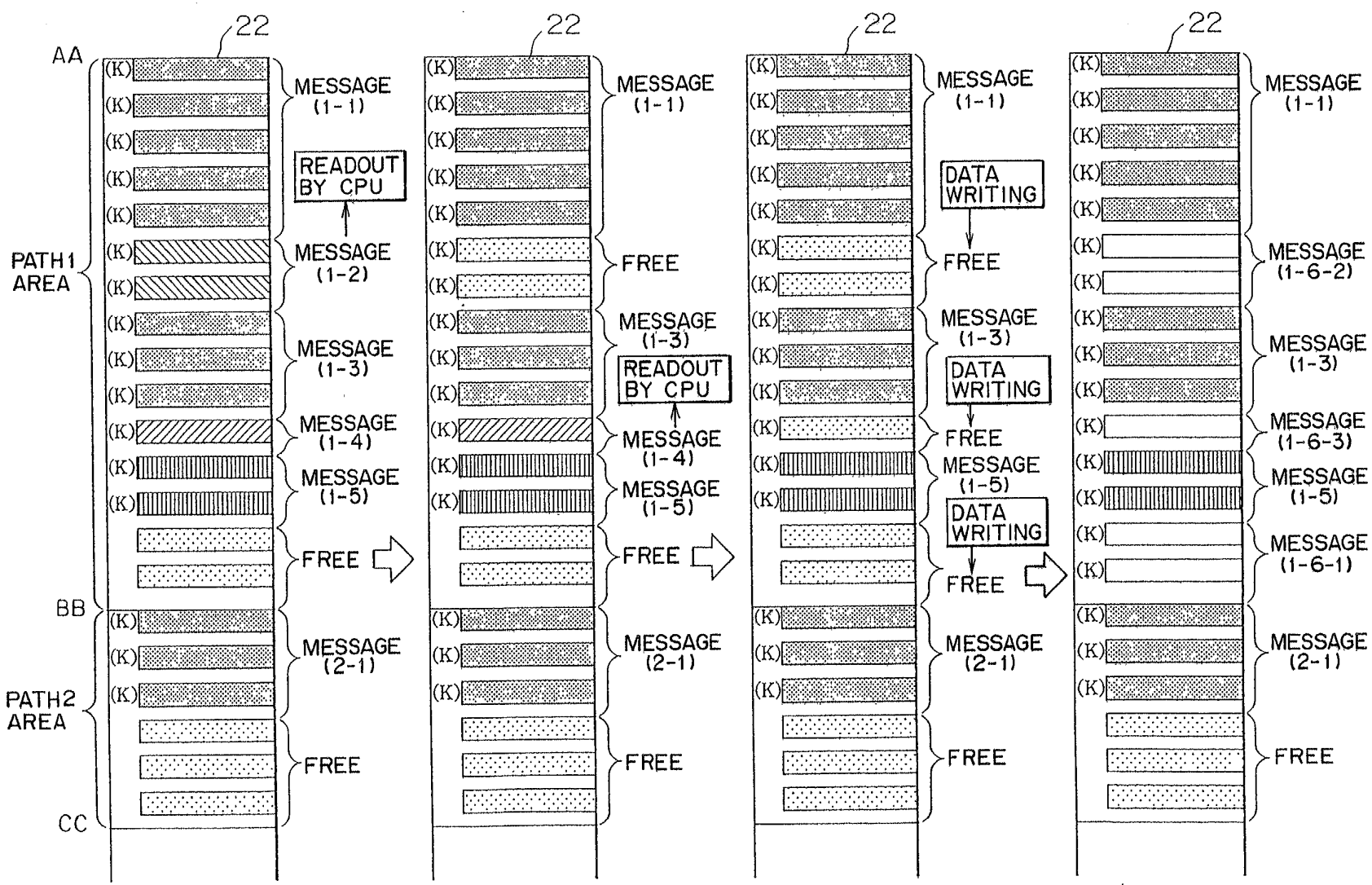


FIG.10(a) FIG.10(b) FIG.10(c) FIG.10(d)



(K) : STORED FLAG

FIG.11(a)

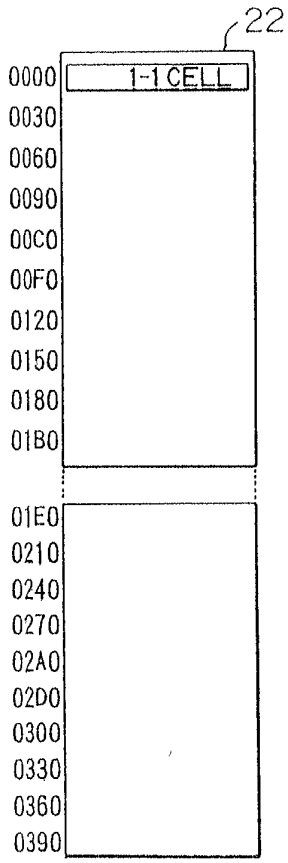


FIG.11(b)

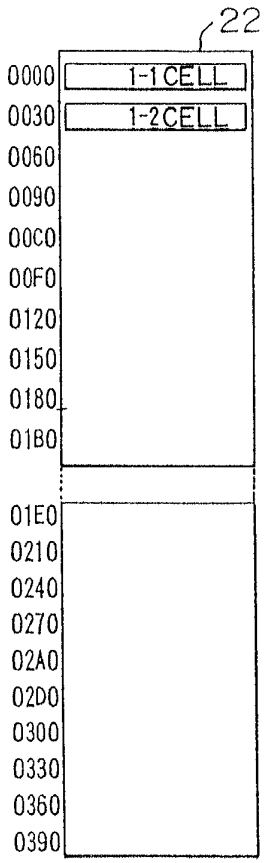


FIG.11(c)

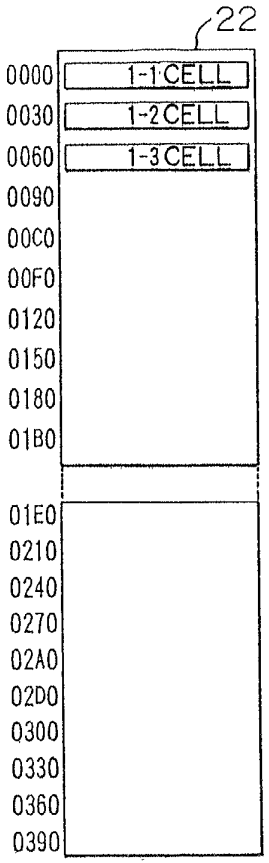


FIG.11(d)

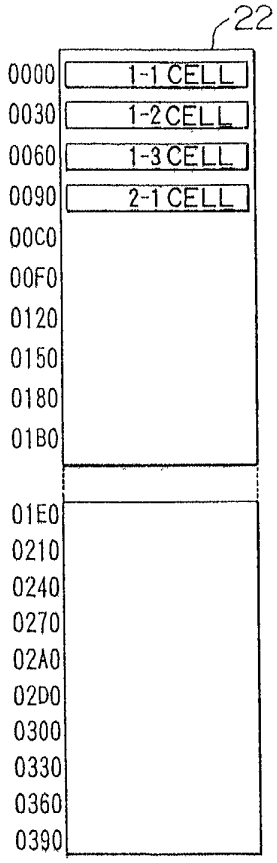


FIG.11(e)

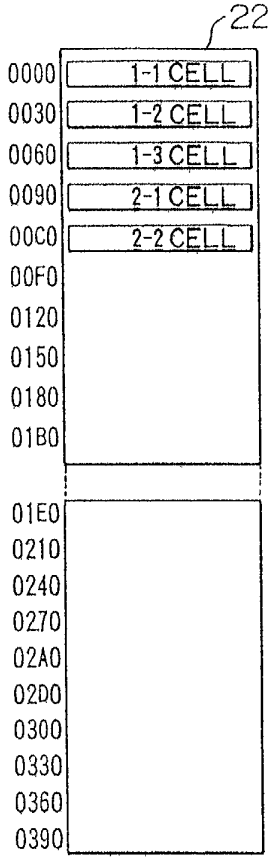


FIG.11(f)

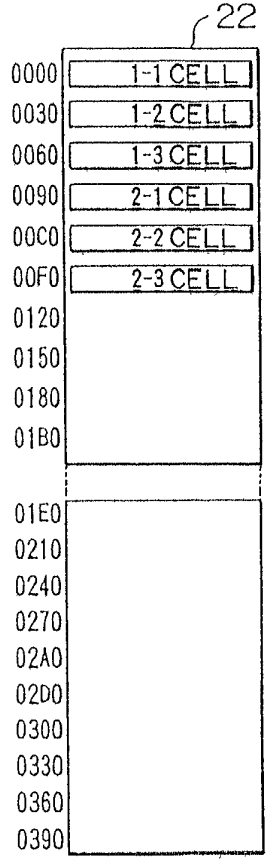


FIG. 12(a)

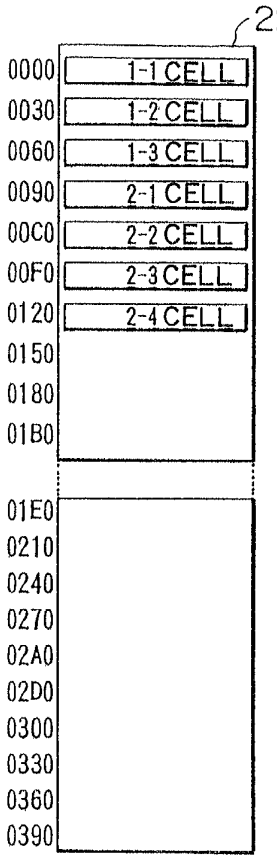


FIG. 12(b)

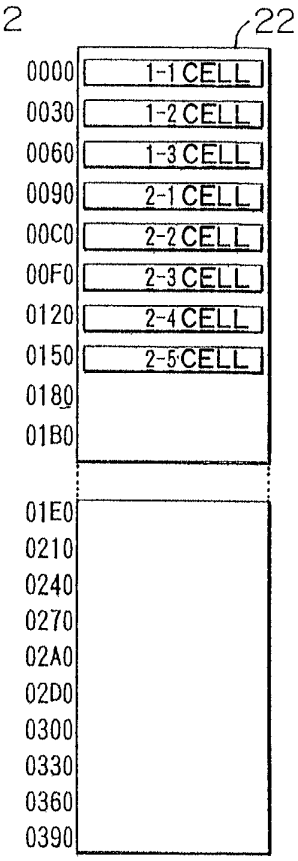


FIG. 12(c)

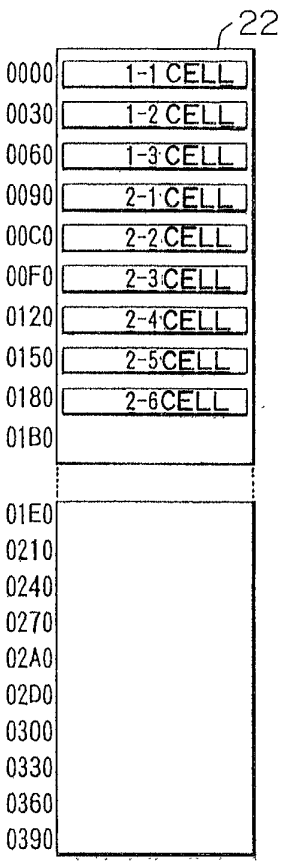


FIG. 12(d)

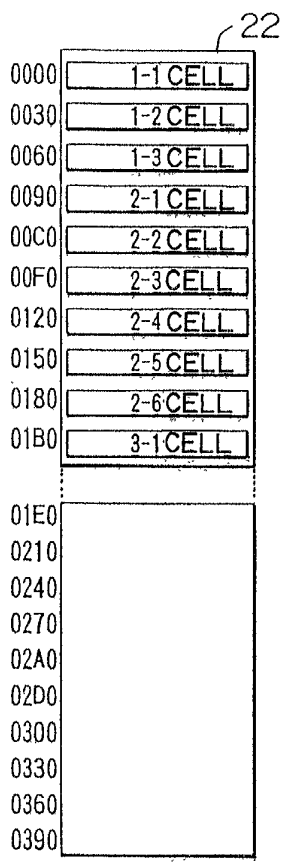


FIG. 12(e)

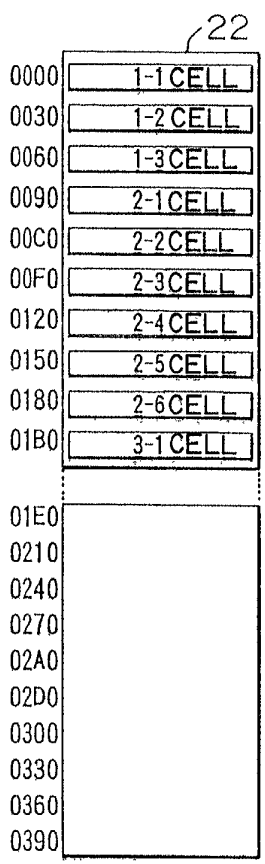


FIG. 12(f)

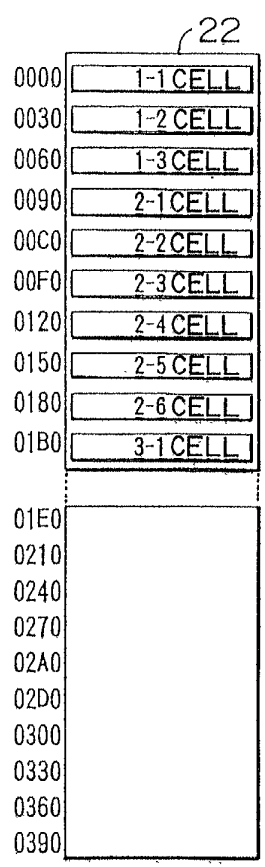


FIG. 13(a)

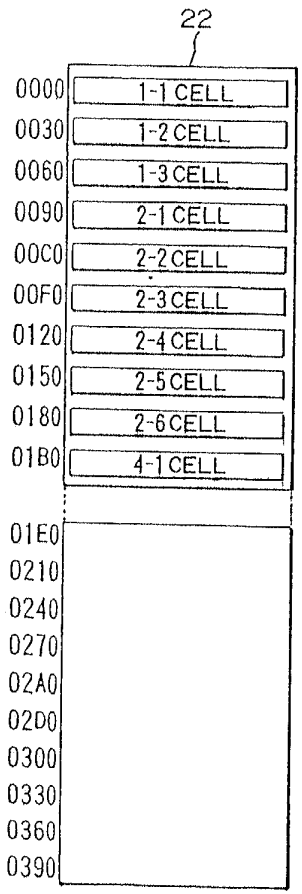


FIG. 13(b)

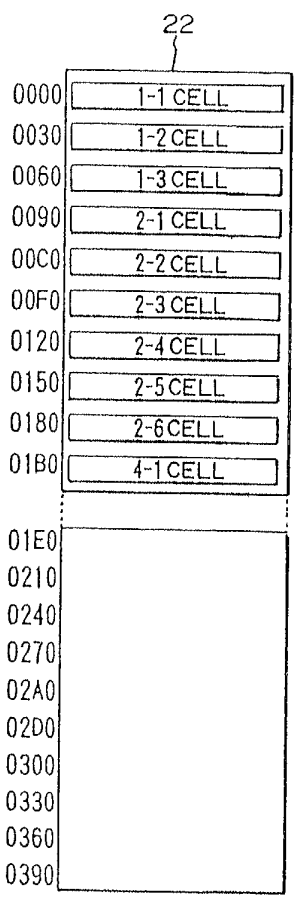


FIG. 13(c)

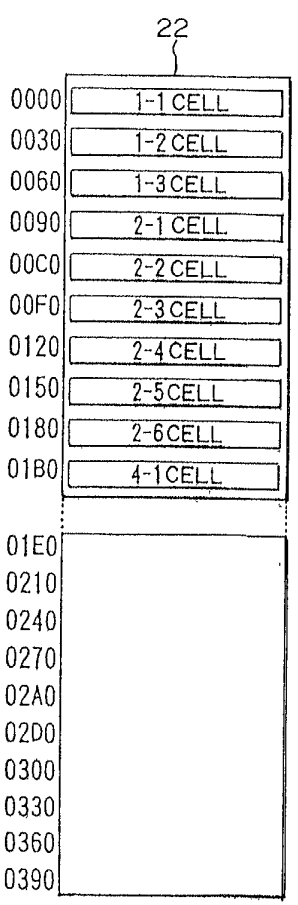


FIG. 13(d)

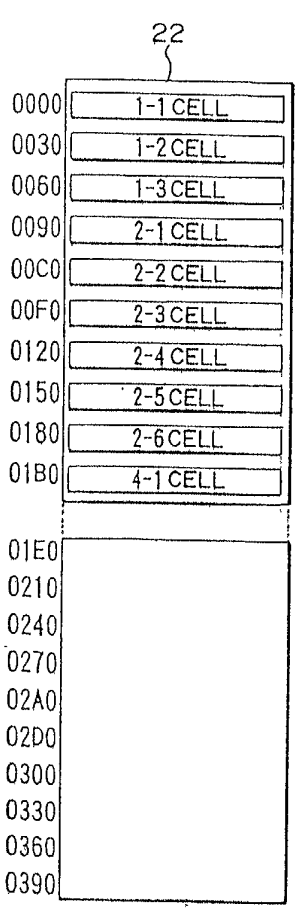


FIG. 13(e)

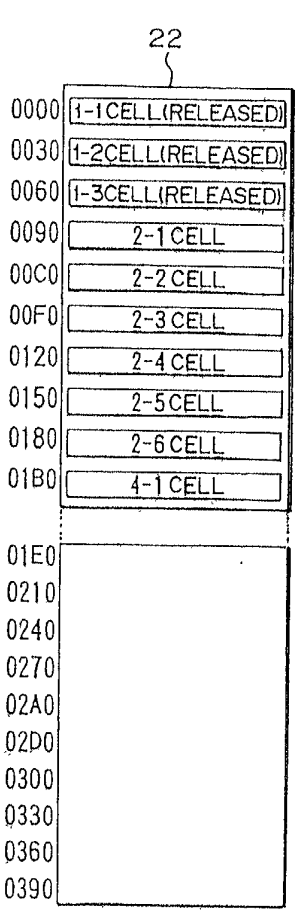


FIG. 13(f)

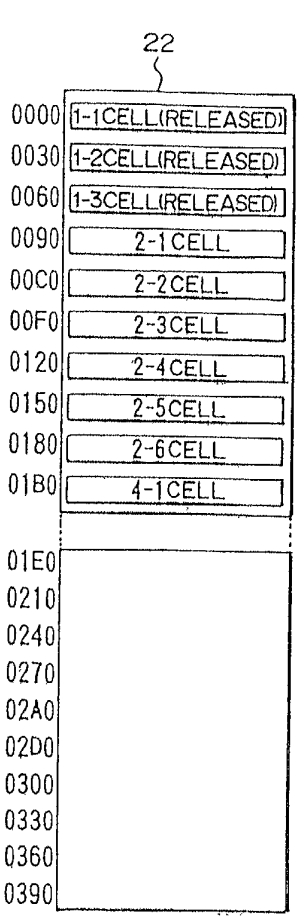


FIG. 14(a)

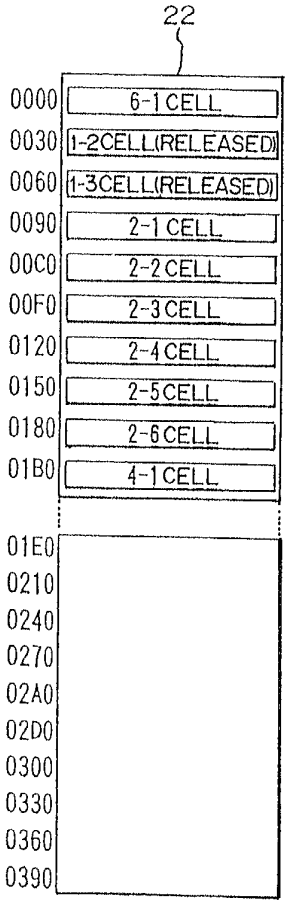


FIG. 14(b)

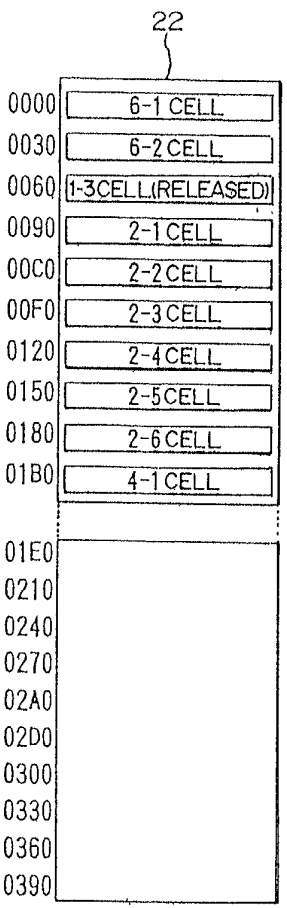


FIG. 14(c)

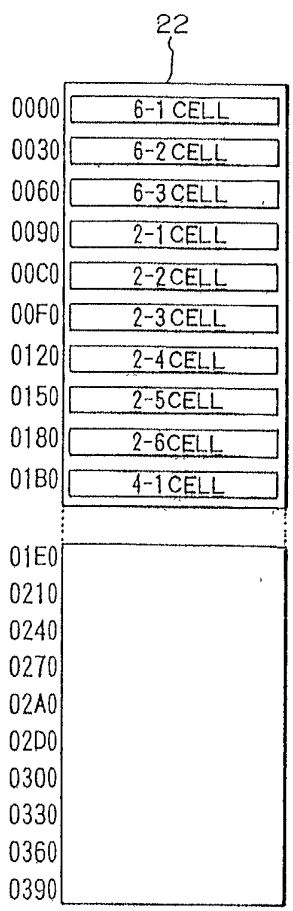


FIG. 14(d)

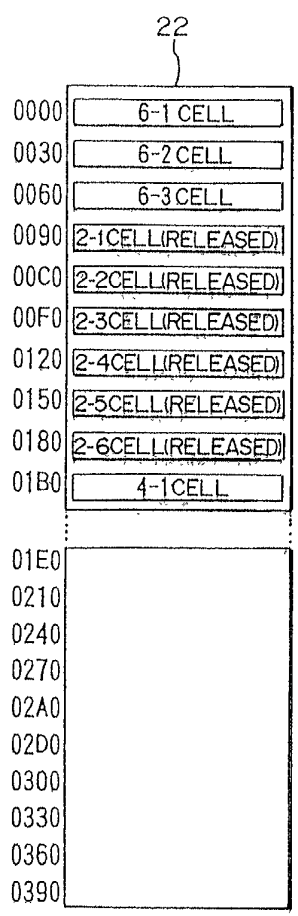


FIG. 14(e)

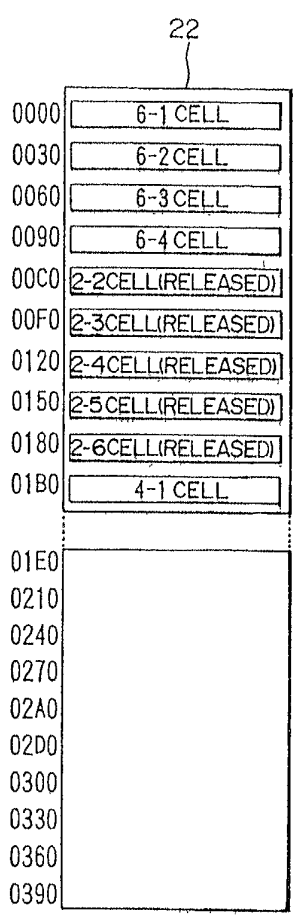


FIG. 14(f)

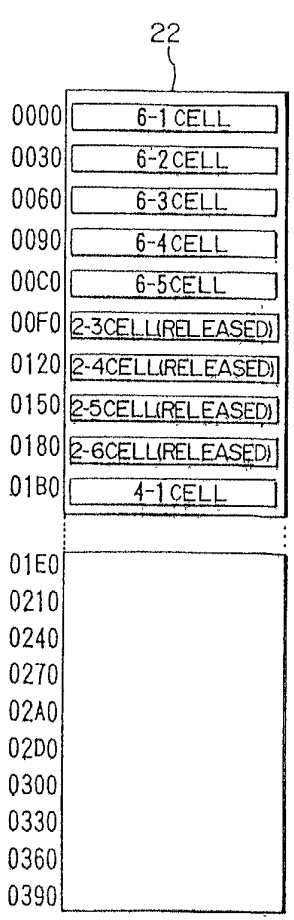


FIG.15(a)

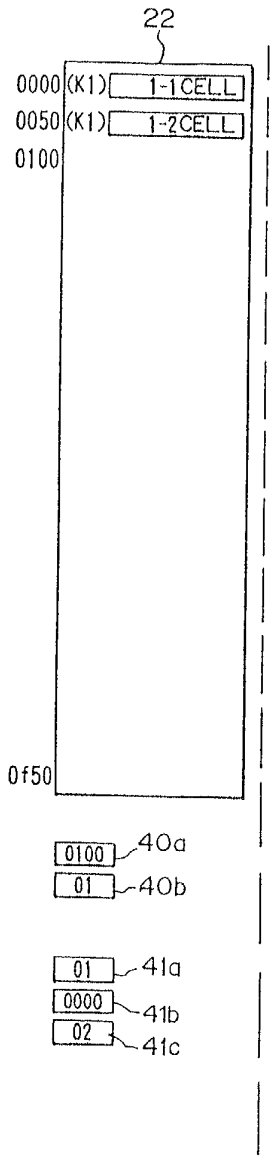


FIG.15(b)

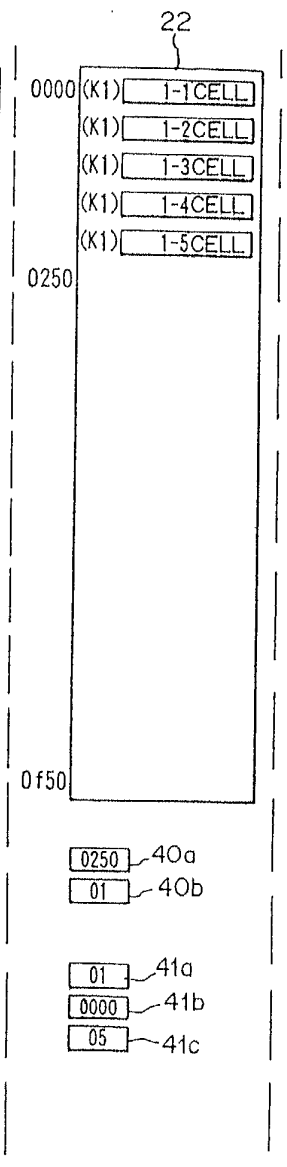


FIG.15(c)

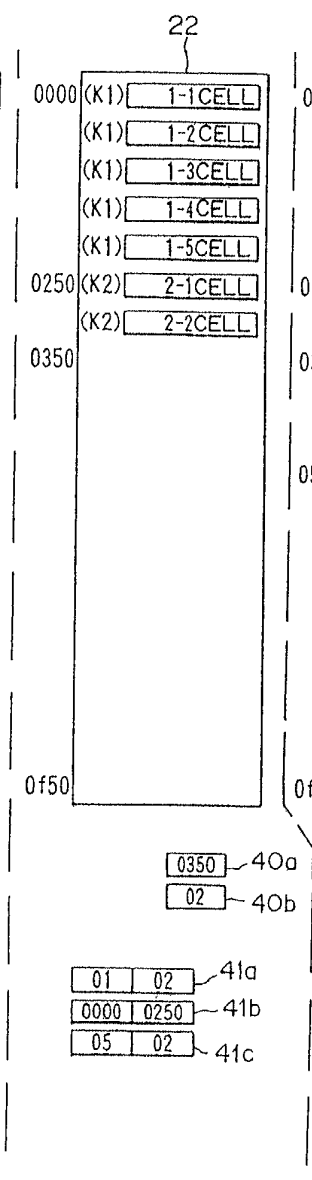


FIG.15(d)

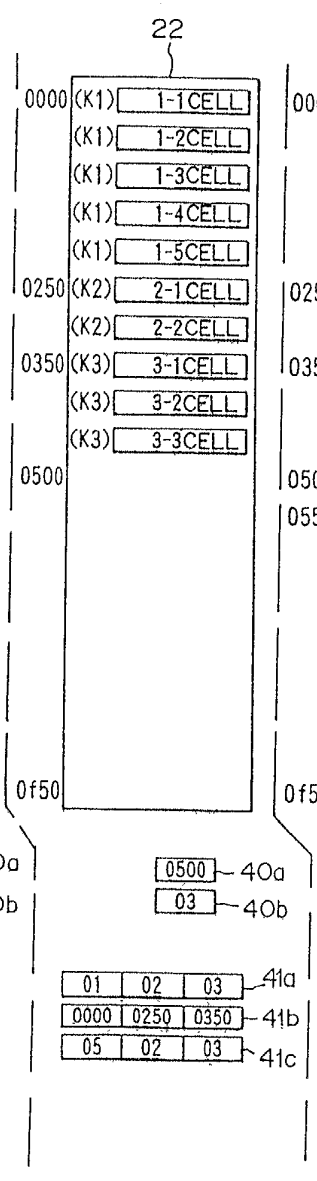


FIG.15(e)

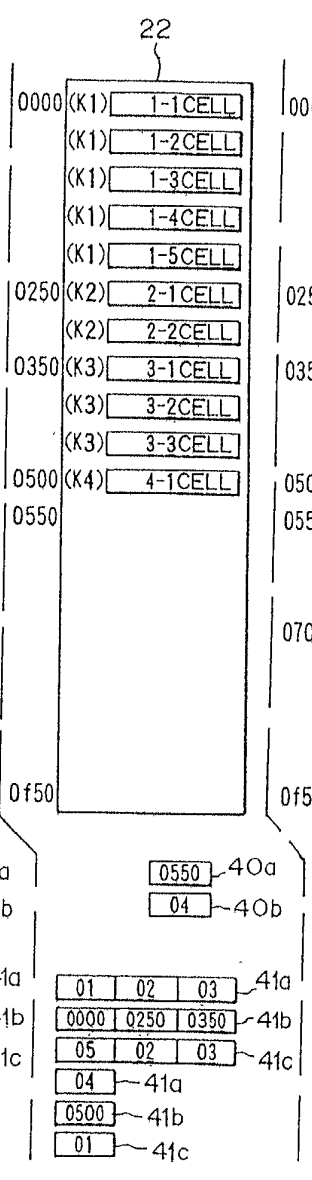


FIG.15(f)

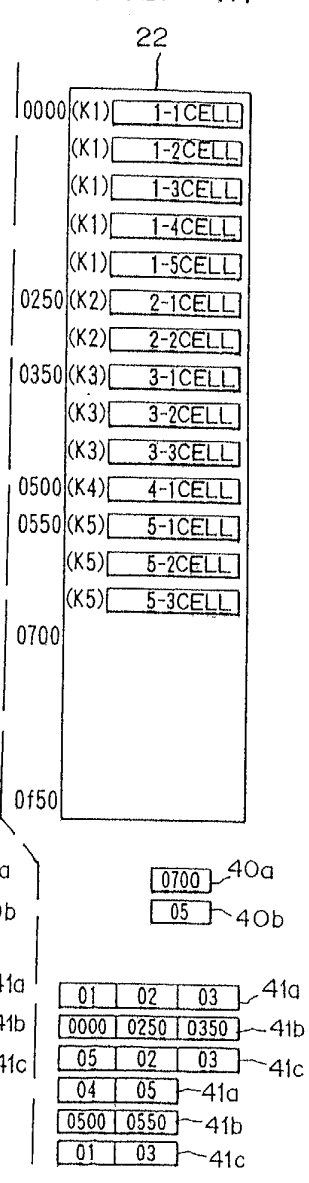


FIG.16(a)

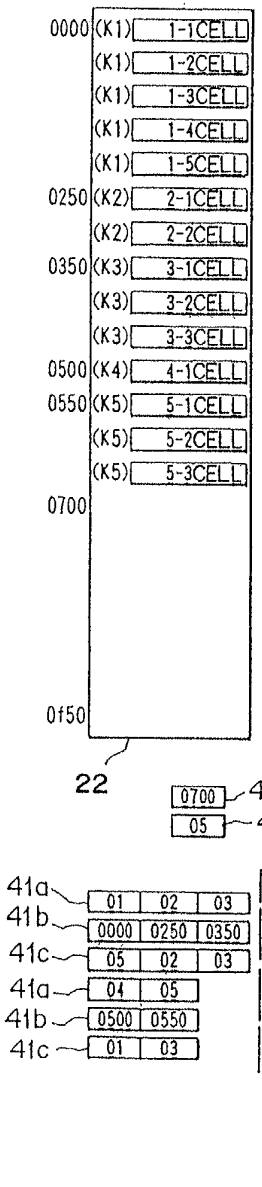


FIG.16(b)

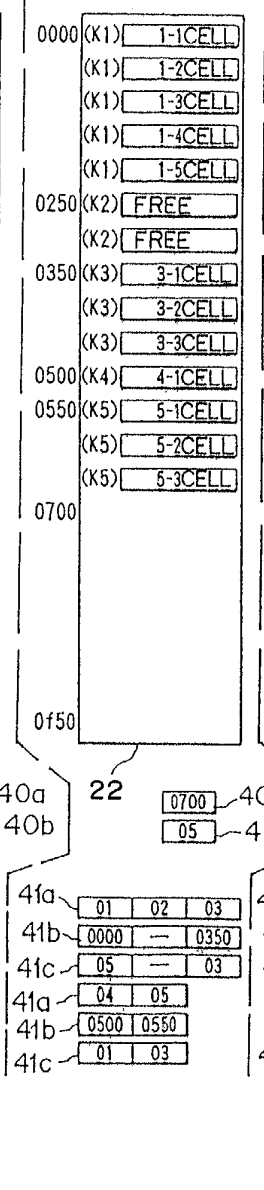


FIG.16(c)

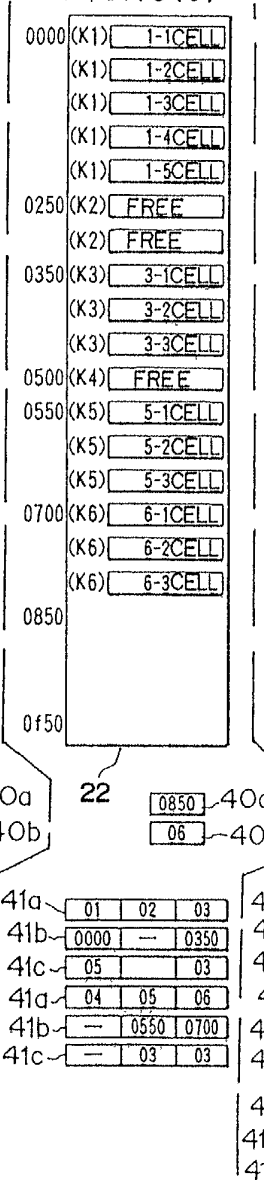


FIG.16(d)

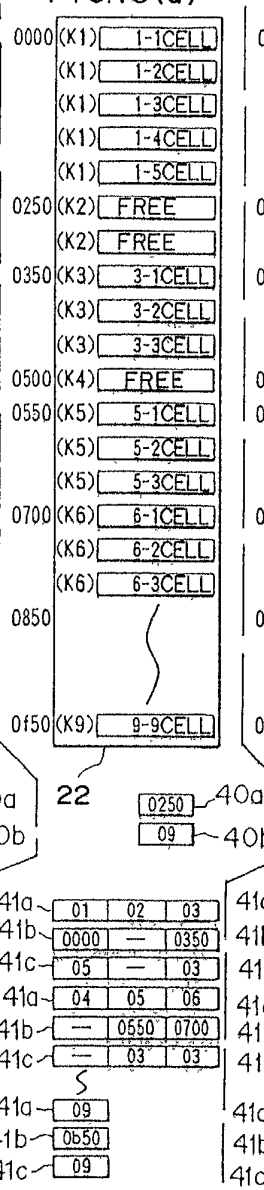


FIG.16(e)

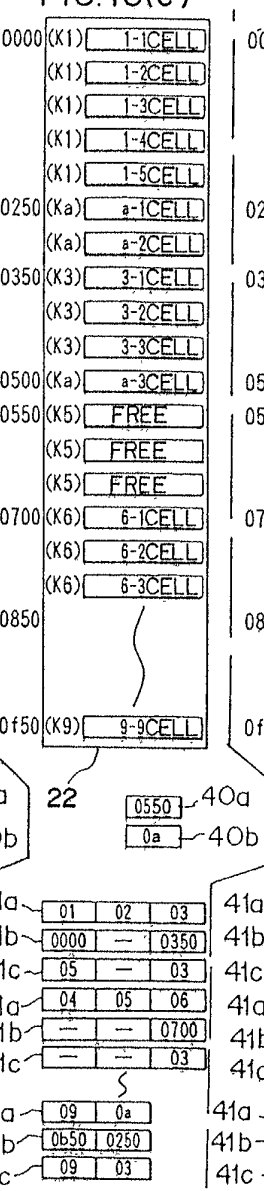


FIG.16(f)

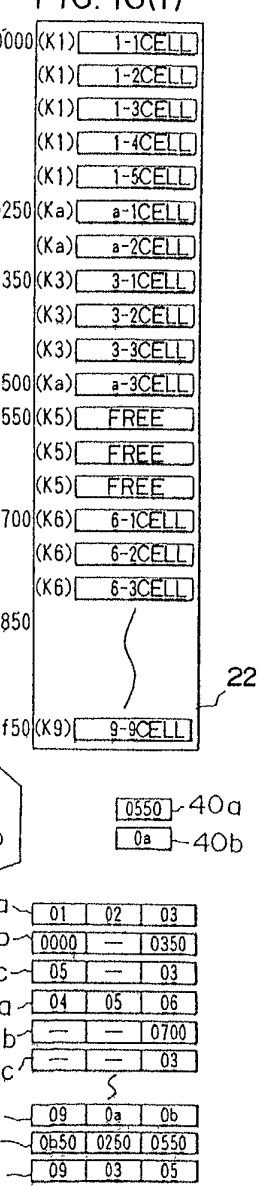


FIG. 17

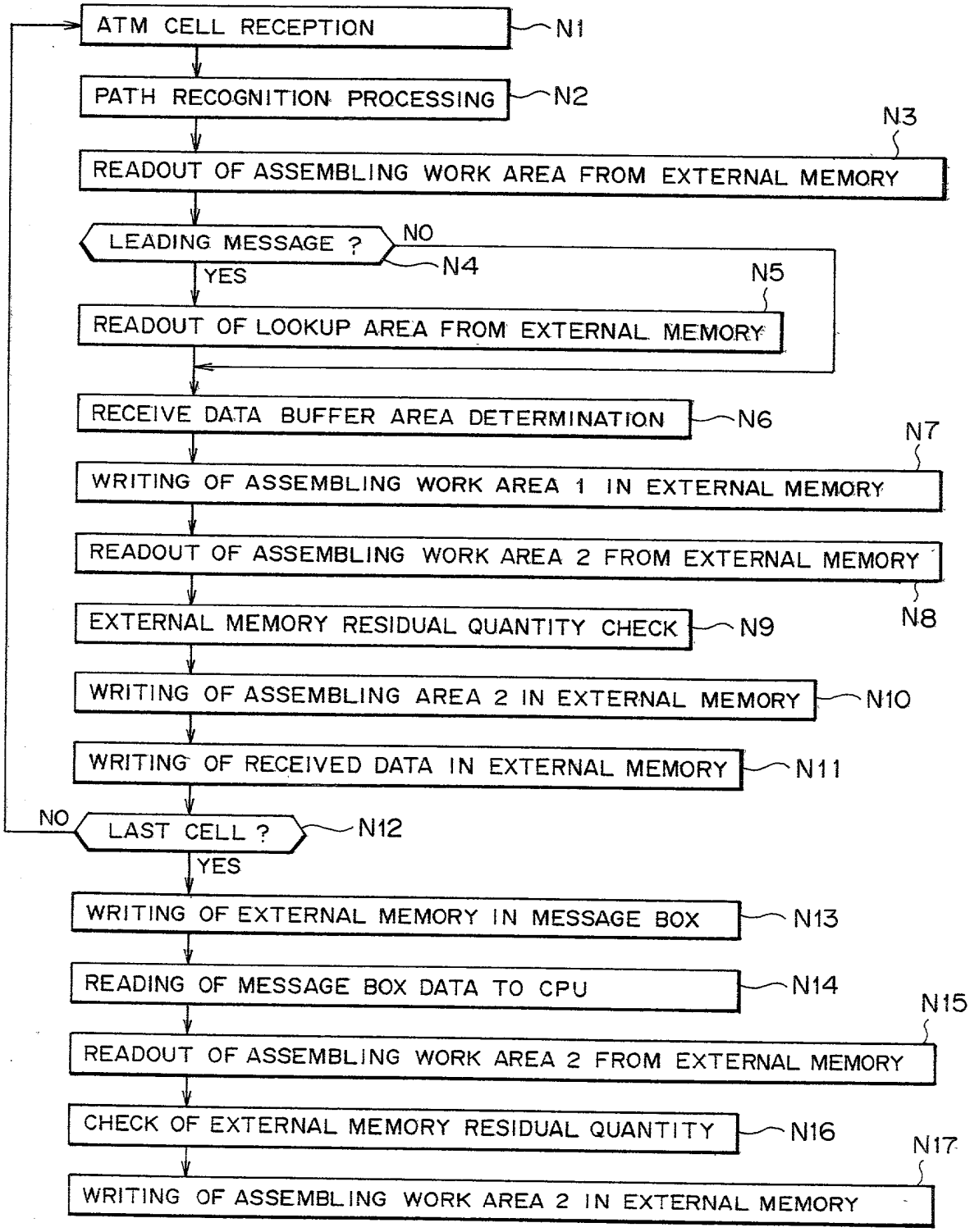

ATM CELL RECEPTION
N1
PATH RECOGNITION PROCESSING
N2
N3
READOUT OF ASSEMBLING WORK AREA FROM EXTERNAL MEMORY
LEADING MESSAGE ?
NO
N4
YES
N5
READOUT OF LOOKUP AREA FROM EXTERNAL MEMORY
RECEIVE DATA BUFFER AREA DETERMINATION
N6
N7
WRITING OF ASSEMBLING WORK AREA 1 IN EXTERNAL MEMORY
READOUT OF ASSEMBLING WORK AREA 2 FROM EXTERNAL MEMORY
N8
EXTERNAL MEMORY RESIDUAL QUANTITY CHECK
N9
WRITING OF ASSEMBLING AREA 2 IN EXTERNAL MEMORY
N10
WRITING OF RECEIVED DATA IN EXTERNAL MEMORY
N11
NO
LAST CELL ?
N12
YES
WRITING OF EXTERNAL MEMORY IN MESSAGE BOX
N13
READING OF MESSAGE BOX DATA TO CPU
N14
N15
READOUT OF ASSEMBLING WORK AREA 2 FROM EXTERNAL MEMORY
CHECK OF EXTERNAL MEMORY RESIDUAL QUANTITY
N16
N17
WRITING OF ASSEMBLING WORK AREA 2 IN EXTERNAL MEMORY

FIG. 18

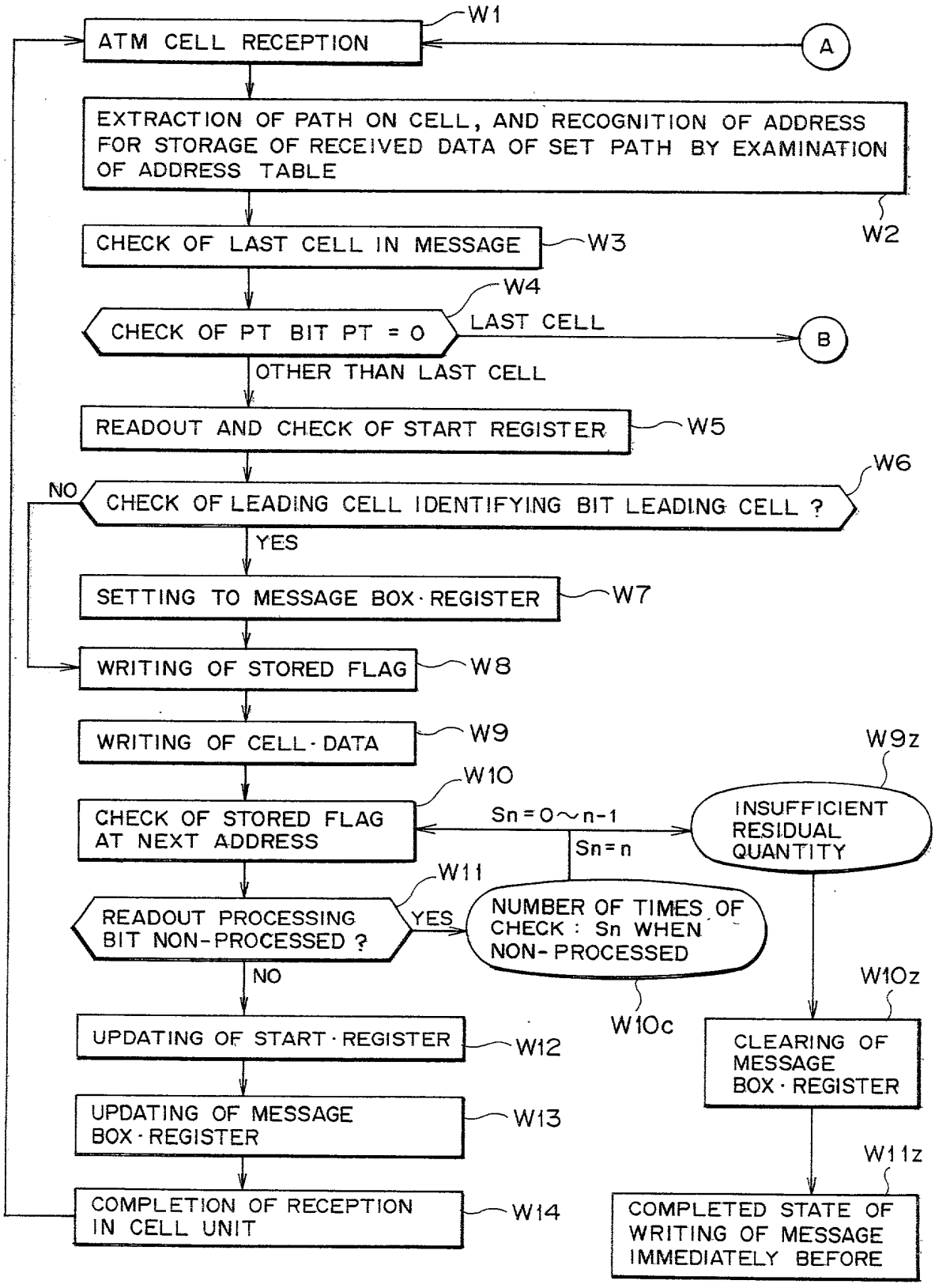

W1
ATM CELL RECEPTION
A
EXTRACTION OF PATH ON CELL, AND RECOGNITION OF ADDRESS FOR STORAGE OF RECEIVED DATA OF SET PATH BY EXAMINATION OF ADDRESS TABLE
W2
CHECK OF LAST CELL IN MESSAGE
W3
W4
CHECK OF PT BIT PT = 0
LAST CELL
B
OTHER THAN LAST CELL
READOUT AND CHECK OF START REGISTER
W5
W6
NO
CHECK OF LEADING CELL IDENTIFYING BIT LEADING CELL ?
YES
SETTING TO MESSAGE BOX · REGISTER
W7
WRITING OF STORED FLAG
W8
WRITING OF CELL · DATA
W9
W9z
W10
CHECK OF STORED FLAG AT NEXT ADDRESS
Sn = 0 ~ n-1
INSUFFICIENT RESIDUAL QUANTITY
Sn = n
W11
READOUT PROCESSING BIT NON-PROCESSED ?
YES
NUMBER OF TIMES OF CHECK : Sn WHEN NON-PROCESSED
W10c
NO
W10z
UPDATING OF START · REGISTER
W12
CLEARING OF MESSAGE BOX · REGISTER
UPDATING OF MESSAGE BOX · REGISTER
W13
W11z
COMPLETION OF RECEPTION IN CELL UNIT
W14
COMPLETED STATE OF WRITING OF MESSAGE IMMEDIATELY BEFORE

FIG. 19

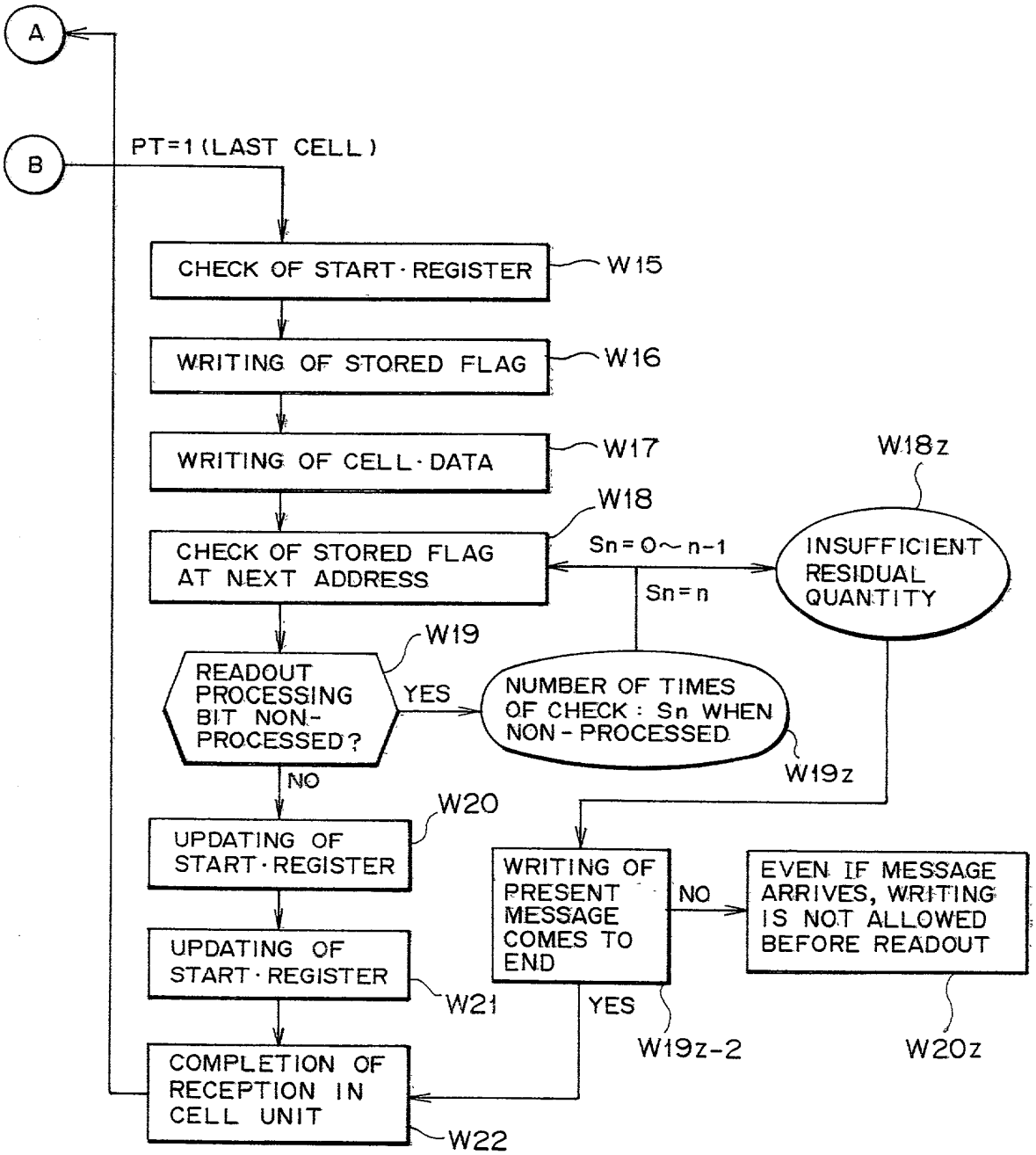

A
B
PT=1 (LAST CELL)
CHECK OF START · REGISTER
W15
WRITING OF STORED FLAG
W16
WRITING OF CELL · DATA
W17
W18z
W18
CHECK OF STORED FLAG AT NEXT ADDRESS
Sn = 0 ~ n-1
INSUFFICIENT RESIDUAL QUANTITY
Sn = n
W19
READOUT PROCESSING BIT NON-PROCESSED?
YES
NUMBER OF TIMES OF CHECK : Sn WHEN NON-PROCESSED
W19z
NO
W20
UPDATING OF START · REGISTER
WRITING OF PRESENT MESSAGE COMES TO END
NO
EVEN IF MESSAGE ARRIVES, WRITING IS NOT ALLOWED BEFORE READOUT
UPDATING OF START · REGISTER
W21
YES
W19z-2
W20z
COMPLETION OF RECEPTION IN CELL UNIT
W22

FIG. 20

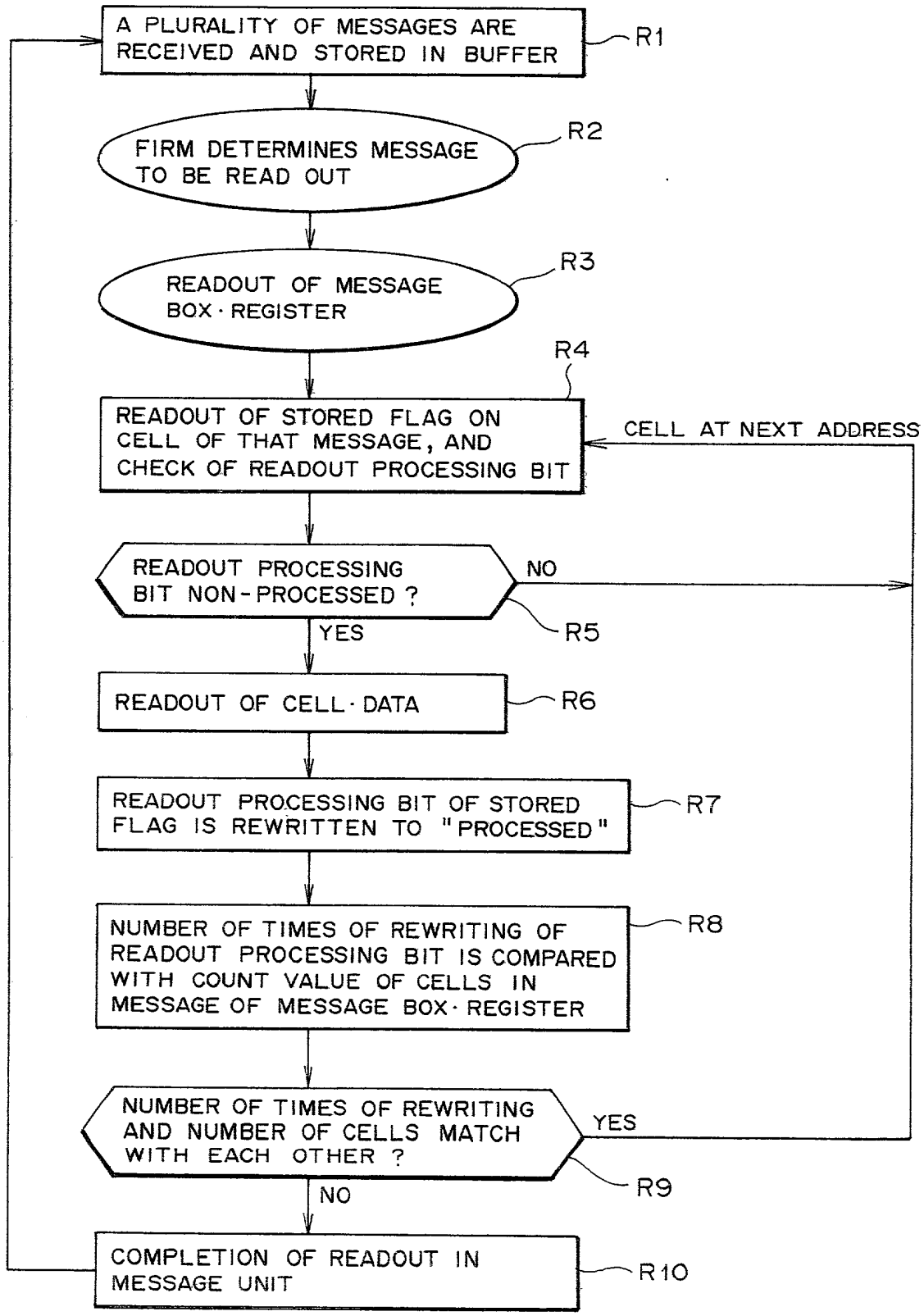

A PLURALITY OF MESSAGES ARE RECEIVED AND STORED IN BUFFER
R1
FIRM DETERMINES MESSAGE TO BE READ OUT
R2
READOUT OF MESSAGE BOX · REGISTER
R3
R4
READOUT OF STORED FLAG ON CELL OF THAT MESSAGE, AND CHECK OF READOUT PROCESSING BIT
CELL AT NEXT ADDRESS
READOUT PROCESSING BIT NON-PROCESSED ?
NO
R5
YES
READOUT OF CELL · DATA
R6
READOUT PROCESSING BIT OF STORED FLAG IS REWRITTEN TO "PROCESSED"
R7
NUMBER OF TIMES OF REWRITING OF READOUT PROCESSING BIT IS COMPARED WITH COUNT VALUE OF CELLS IN MESSAGE OF MESSAGE BOX · REGISTER
R8
NUMBER OF TIMES OF REWRITING AND NUMBER OF CELLS MATCH WITH EACH OTHER ?
YES
R9
NO
COMPLETION OF READOUT IN MESSAGE UNIT
R10

FIG. 21

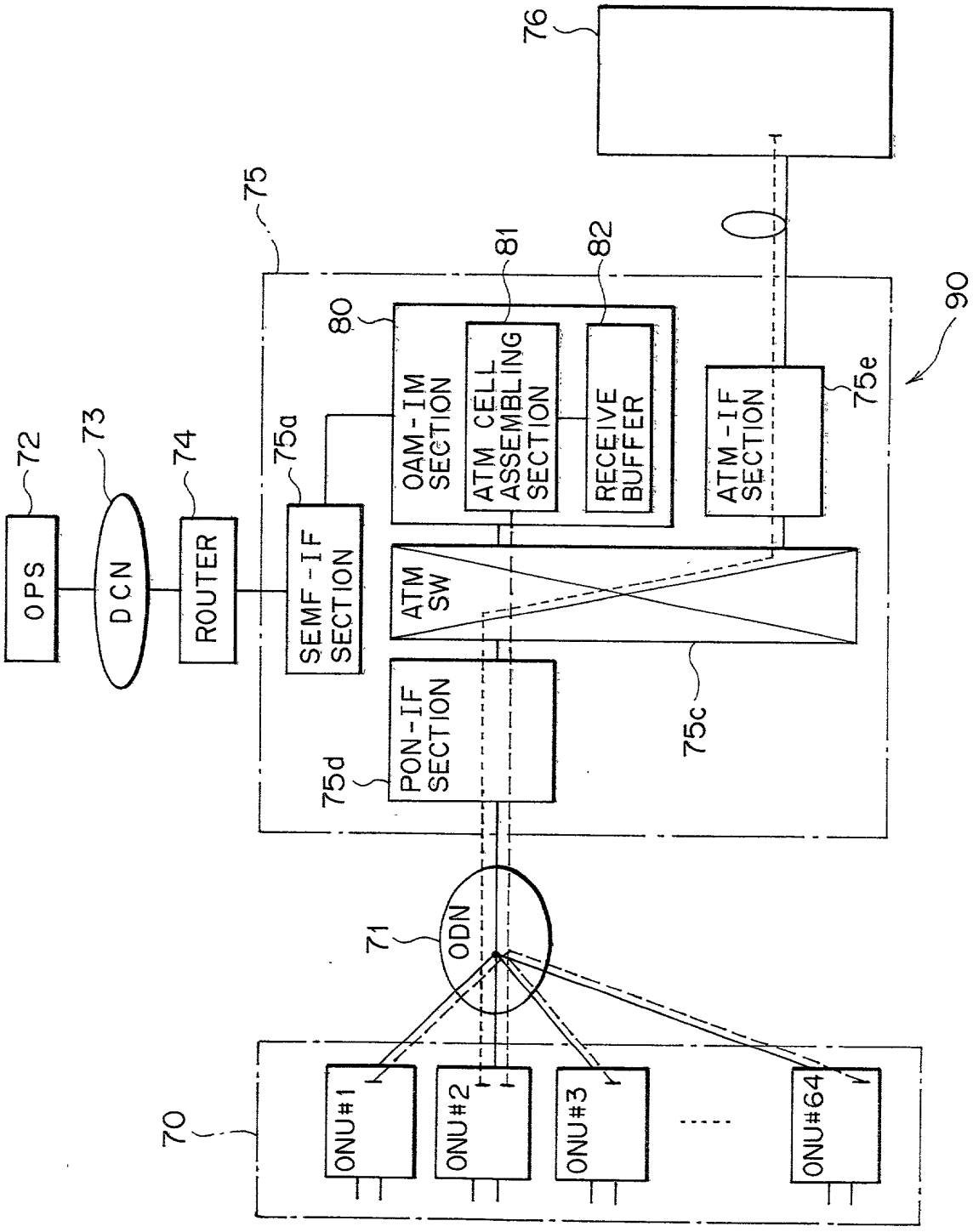

OPS
DCN
ROUTER
SEMF-IF SECTION
OAM-IM SECTION
ATM CELL ASSEMBLING SECTION
RECEIVE BUFFER
ATM-IF SECTION
ATM SW
PON-IF SECTION
ODN
ONU#1
ONU#2
ONU#3
ONU#64
70
71
72
73
74
75
75a
75c
75d
75e
76
80
81
82
90

FIG. 22(a)

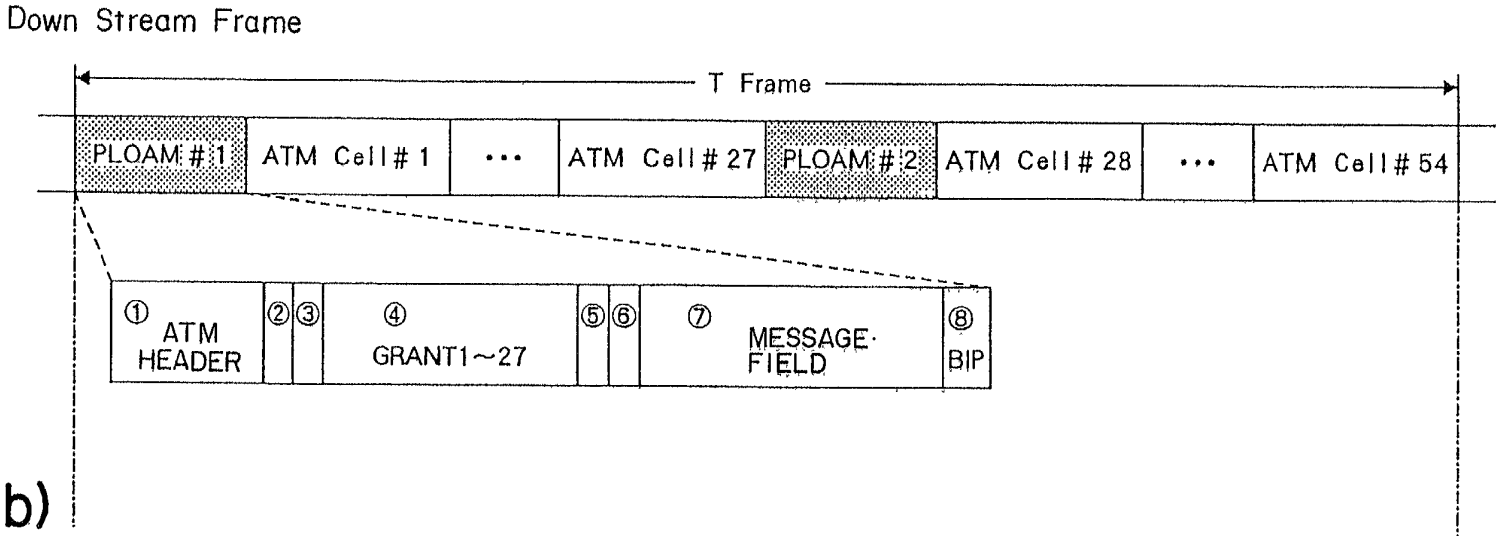


FIG. 22(b)

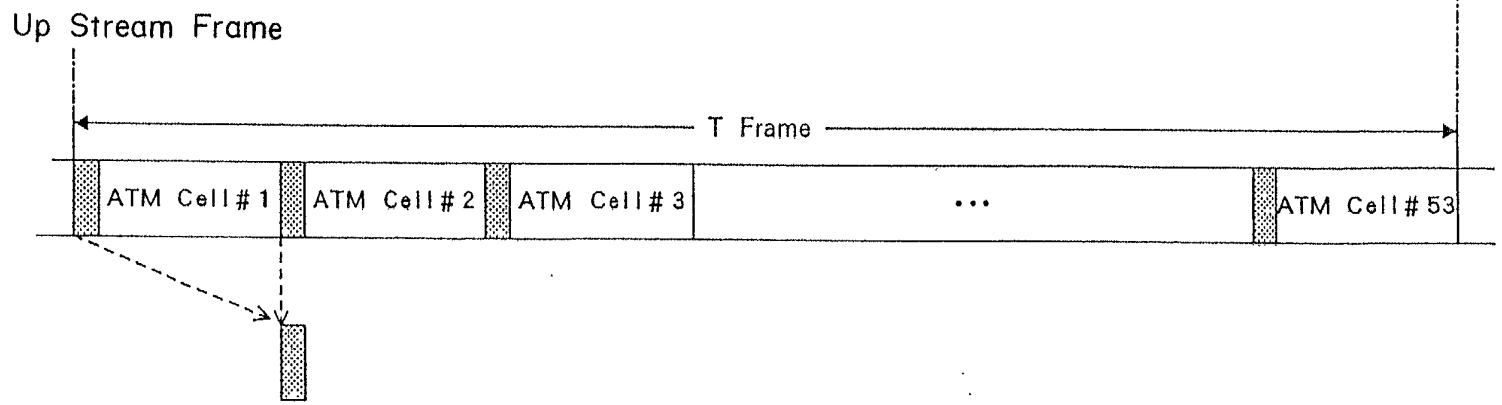


FIG. 23

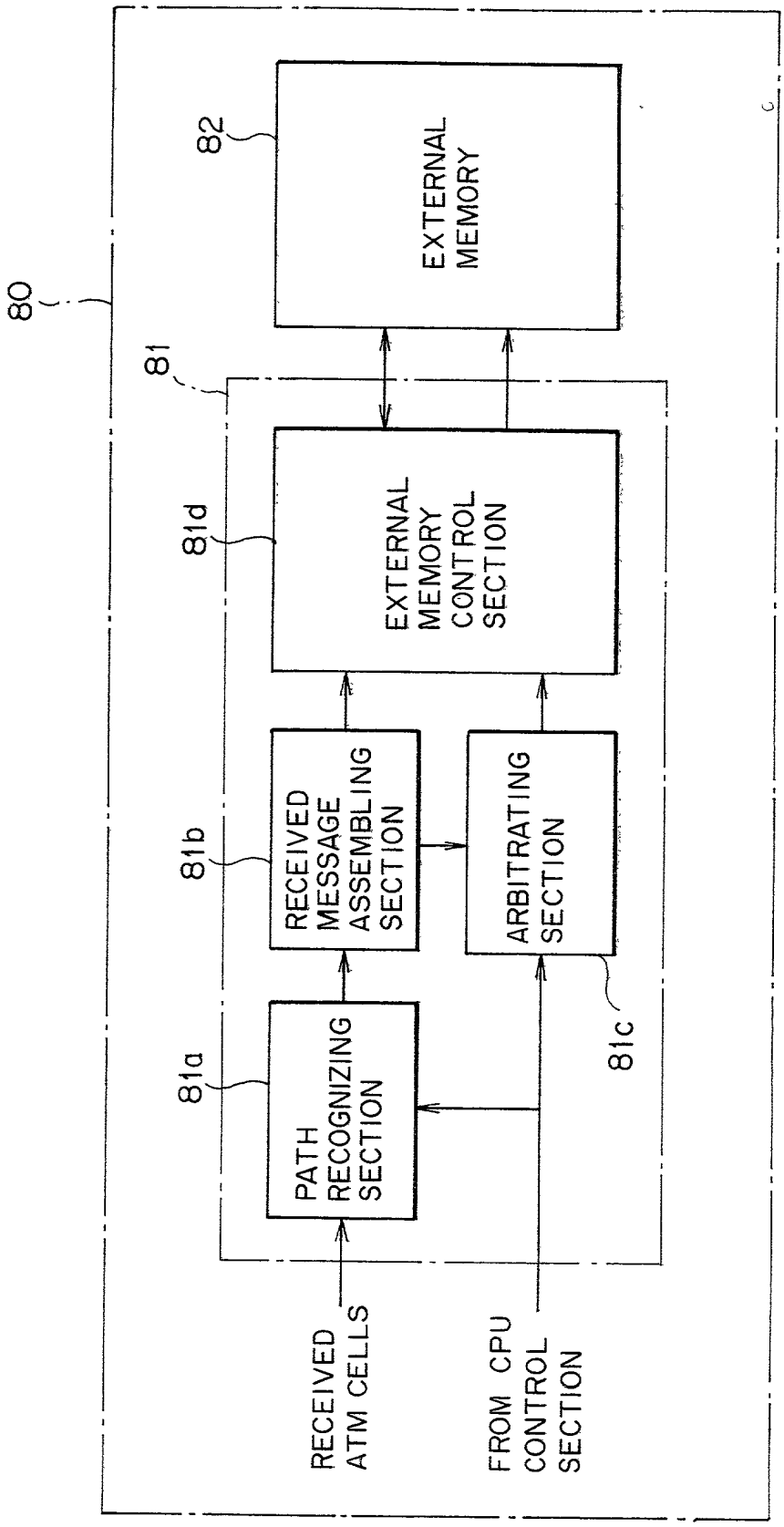

80
82
EXTERNAL MEMORY
81
81d
EXTERNAL MEMORY CONTROL SECTION
81b
RECEIVED MESSAGE ASSEMBLING SECTION
ARBITRATING SECTION
81a
PATH RECOGNIZING SECTION
81c
RECEIVED ATM CELLS
FROM CPU CONTROL SECTION

FIG. 24

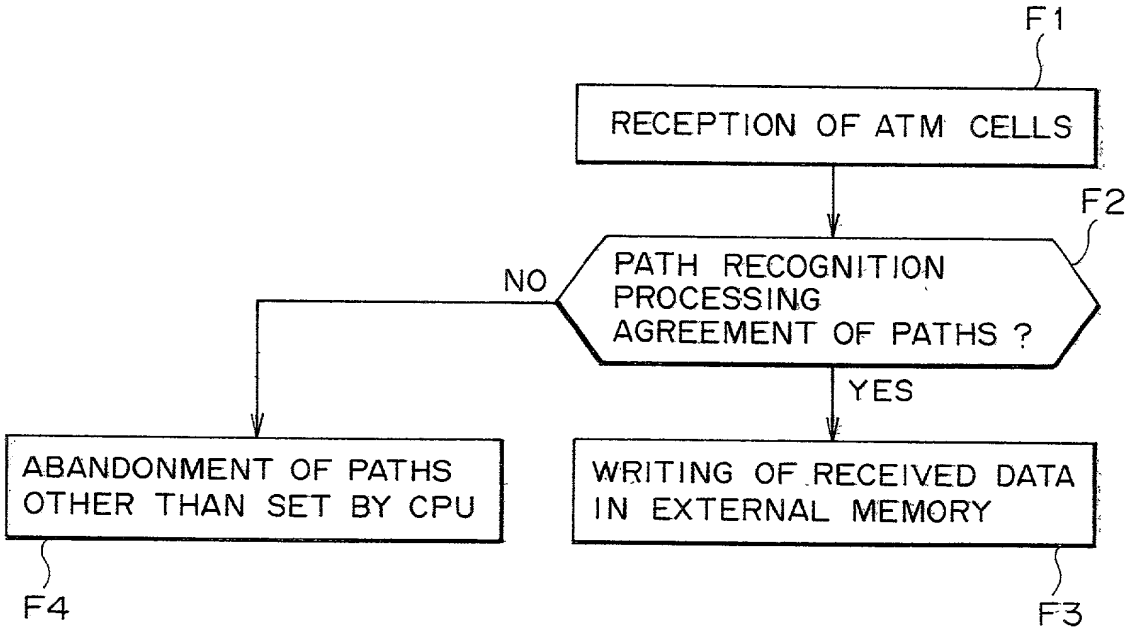

F1
RECEPTION OF ATM CELLS
F2
PATH RECOGNITION PROCESSING AGREEMENT OF PATHS ?
NO
YES
ABANDONMENT OF PATHS OTHER THAN SET BY CPU
WRITING OF RECEIVED DATA IN EXTERNAL MEMORY
F4
F3

FIG. 25

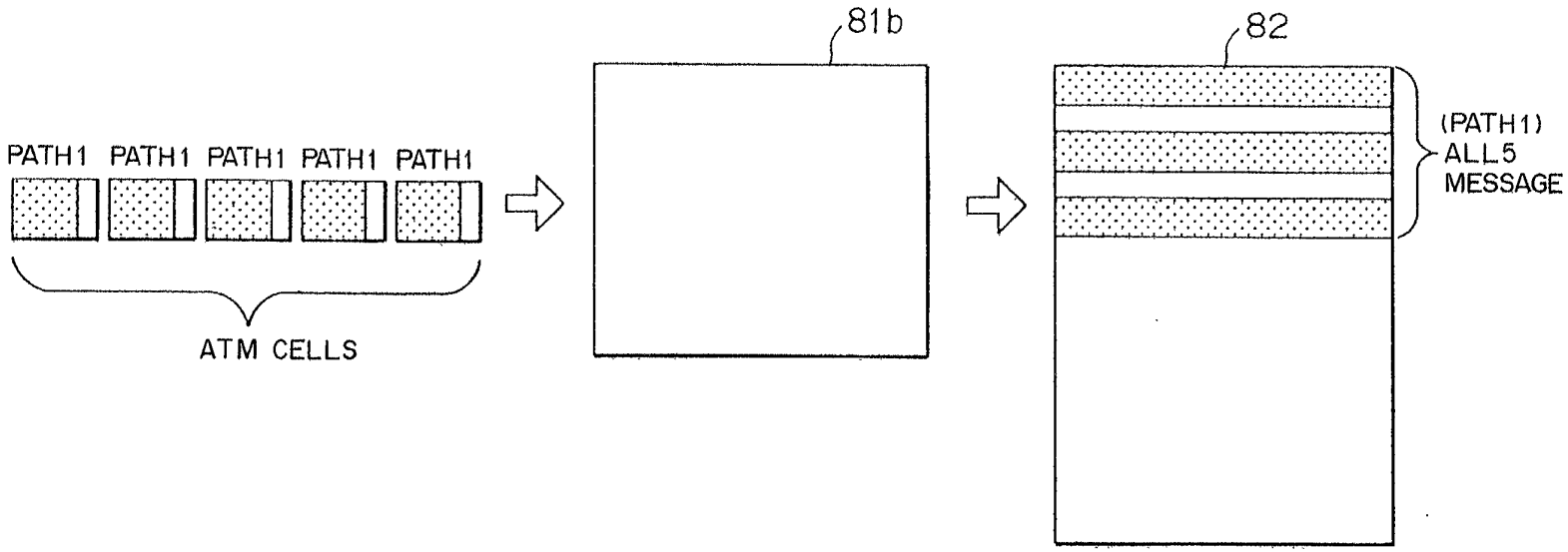

PATH1 PATH1 PATH1 PATH1 PATH1
ATM CELLS
81b
82
(PATH1)
ALL5
MESSAGE

FIG. 26

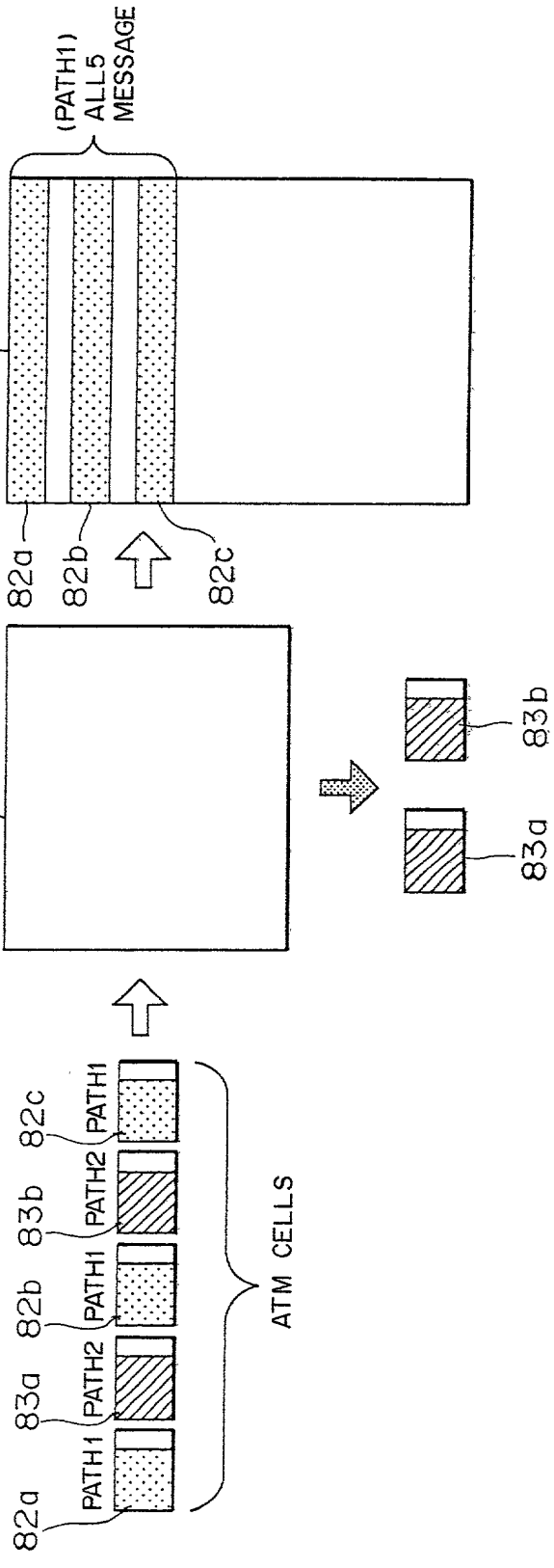
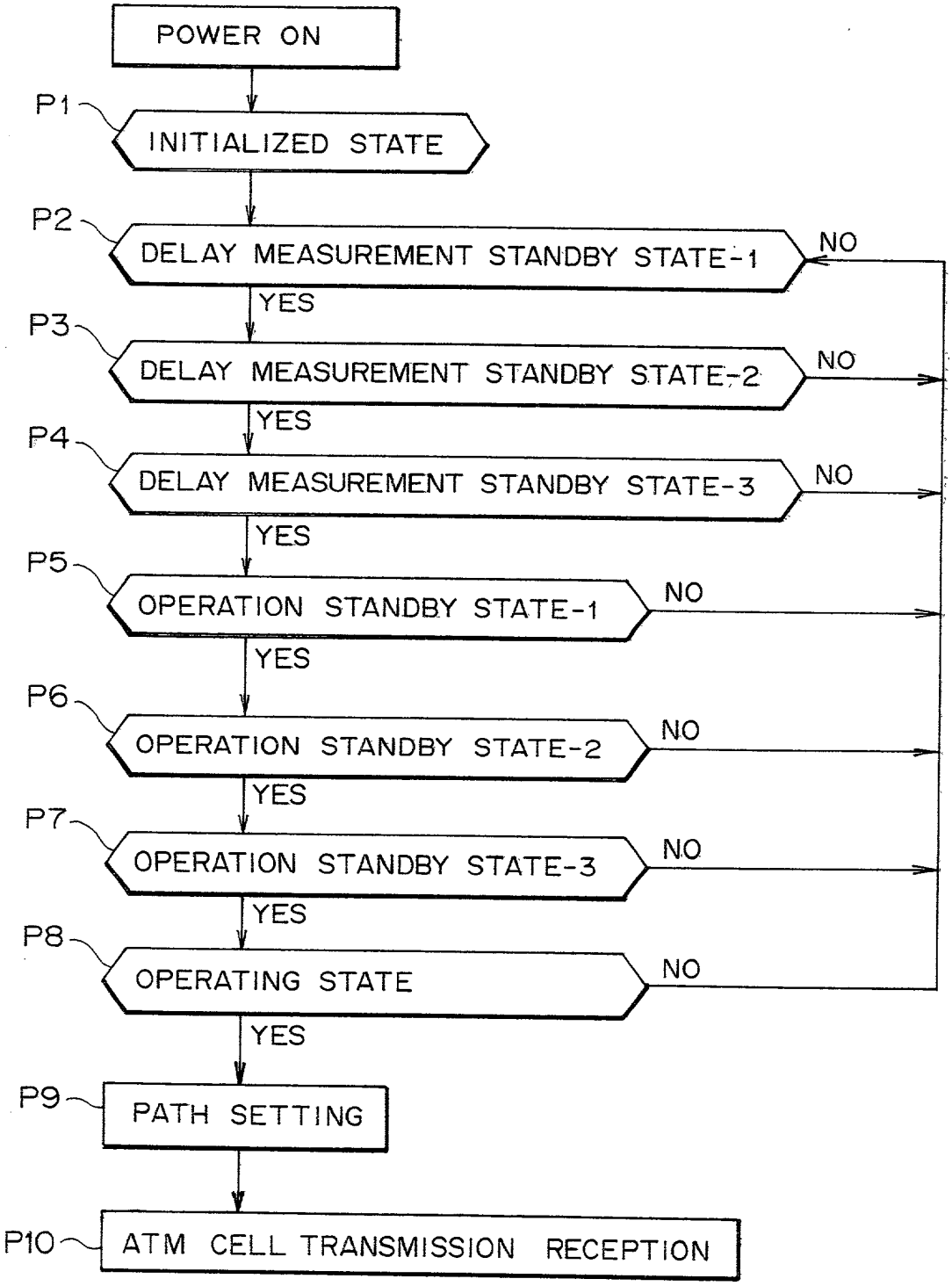

(PATH1)
ALL5
MESSAGE
82
82a
82b
82c
81b
83b
83a
82a
PATH1
83a
PATH2
82b
PATH1
83b
PATH2
82c
PATH1
ATM CELLS

FIG. 27


POWER ON
P1
INITIALIZED STATE
P2
DELAY MEASUREMENT STANDBY STATE-1
NO
YES
P3
DELAY MEASUREMENT STANDBY STATE-2
NO
YES
P4
DELAY MEASUREMENT STANDBY STATE-3
NO
YES
P5
OPERATION STANDBY STATE-1
NO
YES
P6
OPERATION STANDBY STATE-2
NO
YES
P7
OPERATION STANDBY STATE-3
NO
YES
P8
OPERATING STATE
NO
YES
P9
PATH SETTING
P10
ATM CELL TRANSMISSION RECEPTION